General Description

EC2621 Hall-effect sensor is a temperature stable, stress-resistant, Low Tolerance of Sensitivity micro-power switch. Superior high-temperature performance is made possible through a dynamic offset cancellation that utilizes chopper-stabilization. This method reduces the offset voltage normally caused by device over molding, temperature dependencies, and thermal stress.

EC2621 is special made for low operation voltage, 1.65V, to active the chip which is includes the following on a single silicon chip: voltage regulator, Hall voltage generator, small-signal amplifier, chopper stabilization, Schmitt trigger, CMOS output driver. Advanced CMOS wafer fabrication processing is used to take advantage of low-voltage requirements, component matching, Very low input-offset errors, and small component geometries. This device requires the presence of omni-polar magnetic fields for operation.

The package type is in a Halogen Free version has been verified by third party Lab.

Features

- CMOS Hall IC Technology
- Strong RF noise protection
- 1.65 to 3.5V for battery-powered applications
- Omni polar, output switches with absolute value of North or South pole from magnet
- Operation down to 1.65V, Micro power consumption
- High Sensitivity for reed switch replacement applications
- Multi Small Size option
- Low sensitivity drift in crossing of Temp. range
- Ultra Low power consumption at 5uA (Avg)
- High ESD Protection, HMB > ±4KV(min)
- Totem-pole output

Applications

- Solid state switch
- Handheld Wireless Handset Awake Switch (Flip Cell/PHS Phone/Note Book/Flip Video Set)
- Lid close sensor for battery powered devices
- Magnet proximity sensor for reed switch replacement in low duty cycle applications
- Water Meter
- Floating Meter
- PDVD
- NB

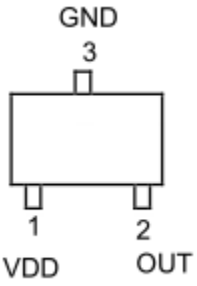
Ordering Information

EC2621 NN XX G R

- R：Tape & Reel
- G：Green package
- Package code:
  - T1：TSOT23-3L
  - BC：SOT553
  - Q1：QFN(2x2)-3L
  - A6：TO92-3L

Type	Part No.	Marking	Marking Information
TSOT23-3L	EC2621NNT1GR	2621 LLLL	LLLL：Lot No
SOT553	EC2621NNBCGR	21YW	YW：Date Code
QFN2x2-3L	EC2621NNQ1GR	21 YW	YW：Date Code
TO92-3L	EC2621NNA6GR	2621 LLLL	LLLL：Lot No

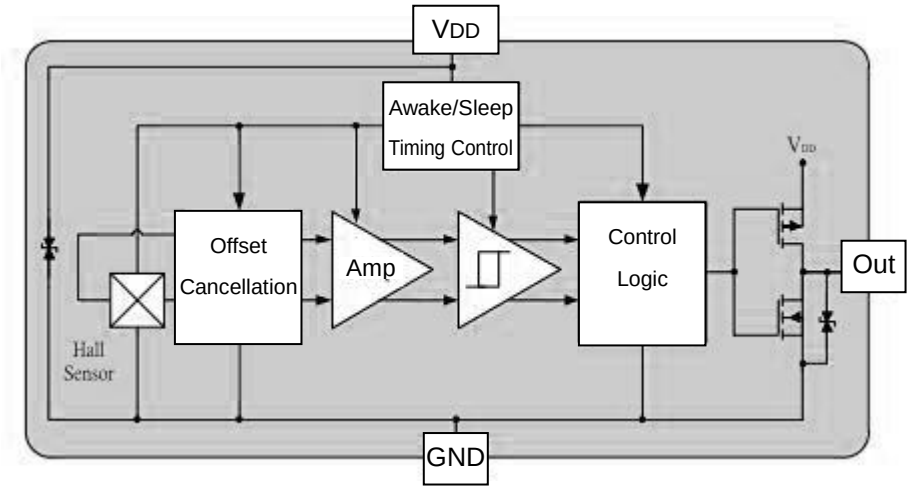
Pin Assignment



Pin Definitions

Pin No.	Symbol	Description
1	VDD	Power Supply Input
2	OUT	Output Pin.
3	GND	Ground Pin

Block Diagram



Note: Static sensitive device; please observe ESD precautions. Reverse V_{DD} protection is not included. For reverse voltage protection, a 100Ω resistor in series with V_{DD} is recommended.

Absolute Maximum Ratings At TA=25℃

Characteristics		Values	Unit
Supply voltage,(V_{DD})		4.5	V
Output Voltage,(V_{OUT})		4.5	V
Reverse Voltage , (V_{DD}) (V_{OUT})		-0.3	V
Magnetic flux density		Unlimited	Gauss
Output current,(I_{OUT})		1	mA
Operating temperature range, (T_A)		-40 to +85	℃
Storage temperature range, (T_S)		-65 to +150	℃
Maximum Junction Temp,(T_J)		150	℃
Supply voltage,(V_{DD})		4.5	V
Output Voltage,(V_{OUT})		4.5	V
Thermal Resistance(θ_{JA})	TSOT23-3L	310	℃/W
	SOT553	540	℃/W
	QFN2x2-3L	206	℃/W
	TO92-3L	543	℃/W
Thermal Resistance(θ_{JC})	TSOT23-3L	223	℃/W
	SOT553	390	℃/W
	QFN2x2-3L	148	℃/W
	TO92-3L	410	℃/W
Package Power Dissipation, (P_D)	TSOT23-3L	400	mW
	SOT223	230	mW
	QFN2x2-3L	606	mW
	TO92-3L	230	mW

Note: Exceeding the absolute maximum ratings may cause permanent damage. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

Electrical Specifications

DC Operating Parameters：T_A=25℃, V_{DD}=1.8V

Parameters	Test Conditions	Min	Typ	Max	Units
Supply Voltage,(V_{DD})	Operating	1.65		3.5	V
Supply Current,(I_{DD})	Awake State		1.4	3	mA
	Sleep State		3.6	7	μA
	Average		5	10	μA
Output Leakage Current,(Ioff)	Output off			1	uA
Output High Voltage,(V_{OH})	I_{OUT}=0.5mA(Source)	V_{DD}-0.12			V
Output Low Voltage,(V_{OL})	I_{OUT}=0.5mA(Sink)			0.12	V
Awake mode time,(T_{AW})	Operating		40	80	uS
Sleep mode time,(T_{SL})	Operating		40	80	mS
Duty Cycle,(D,C)			0.1		%
Electro-Static Discharge	HBM	4			KV

Magnetic Specifications

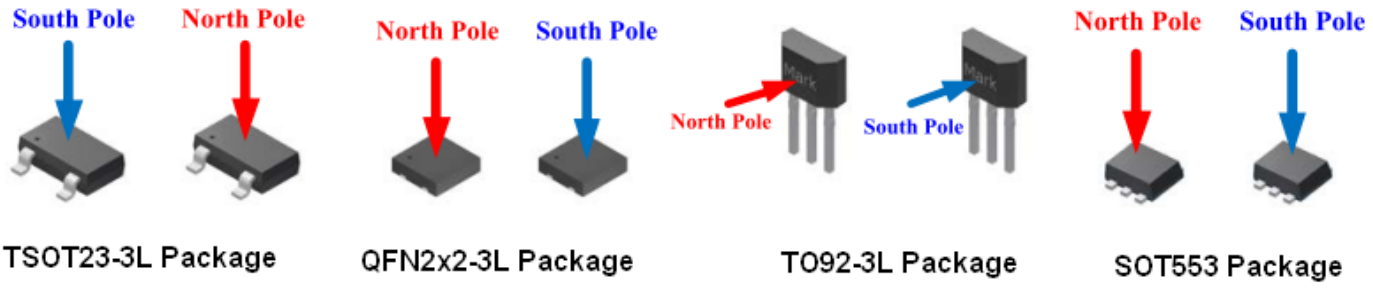
DC Operating Parameters：T_A=25℃, V_{DD}=1.8V

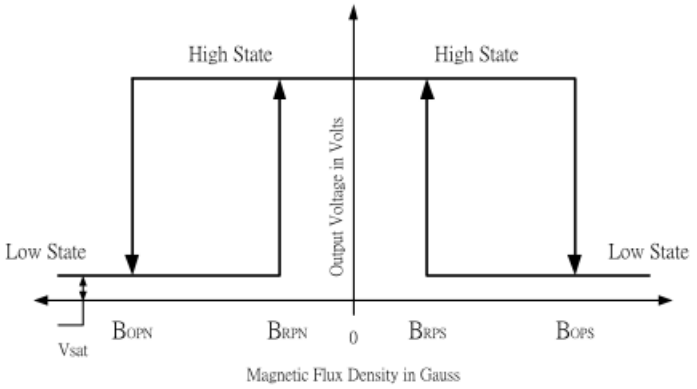
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Operating Point	B_{OPS}	S pole to branded side, B > B_{OP}, Vout On		30	55	Gauss
	B_{OPN}	N pole to branded side, B > B_{OP}, Vout On	-55	-30		Gauss
Release Point	B_{RPS}	S pole to branded side, B < B_{RP}, Vout Off	10	20		Gauss
	B_{RPN}	N pole to branded side, B < B_{RP}, Vout Off		-20	-10	Gauss
Hysteresis	B_{HYS}	|BOPx - BRPx|		10		Gauss

Output Behavior versus Magnetic Polar

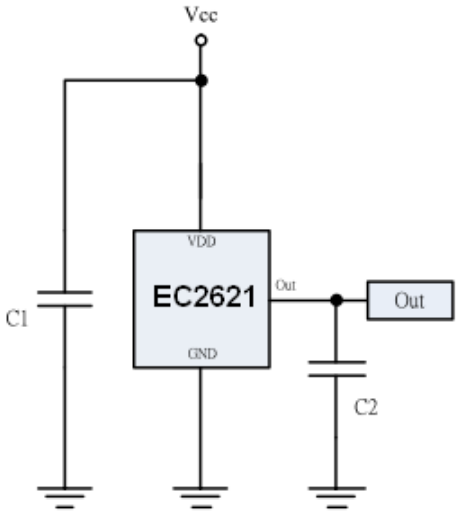
DC Operating Parameters：T_A = -40 to 85℃, V_{DD} =1.8V to 3.5V

Parameter	Test condition	OUT(TSOT23-3L)	Test condition	OUT(SOT553)
South pole	B<Bop[(-55)~(-10)]	Low	B<Bop[(-55)~(-10)]	Low
Null or weak magnetic field	B=0 or B < BRP	High	B=0 or B < BRP	High
North pole	B>Bop(55~10)	Low	B>Bop(55~10)	Low
Parameter	Test condition	OUT(TSOT23-3L)	Test condition	OUT(SOT553)
South pole	B<Bop[(-55)~(-10)]	Low	B<Bop[(-55)~(-10)]	Low





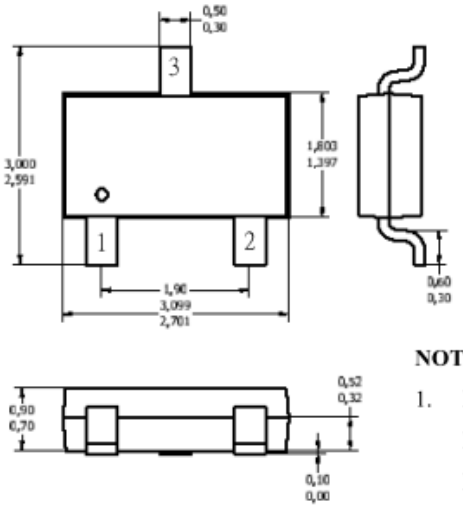
Typical Application circuit



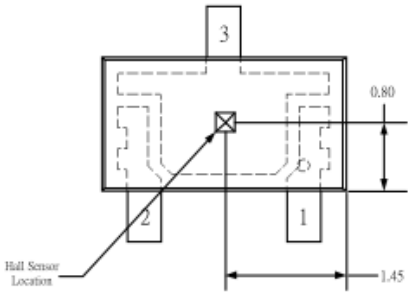
C1 : 10nF
C2 : 100pF

Sensor Location and package dimension

TSOT23-3L Package
(Top View)



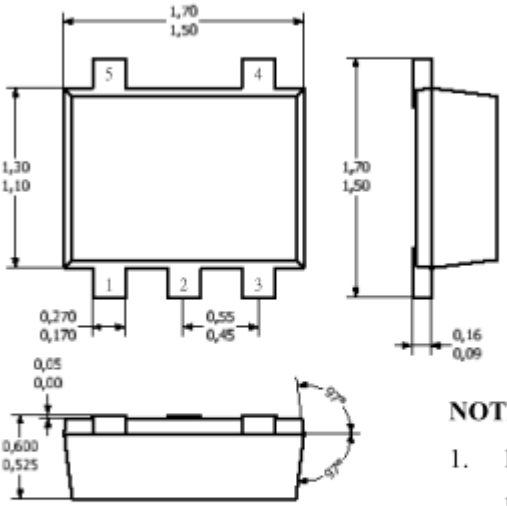
Hall Plate Chip Location
(Bottom view)



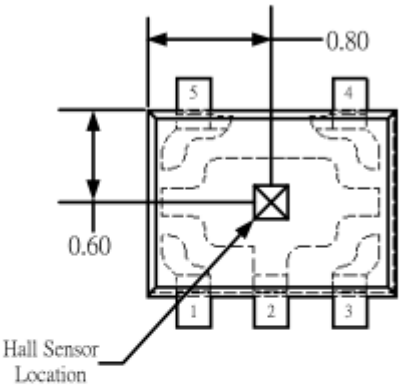
NOTES:

1. PINOUT (See Top View at left:)
   - Pin 1 VDD
   - Pin 2 Output
   - Pin 3 GND
2. Controlling dimension: mm;

SOT553 Package
(Top View)



Hall Plate Chip Location
(Top View)

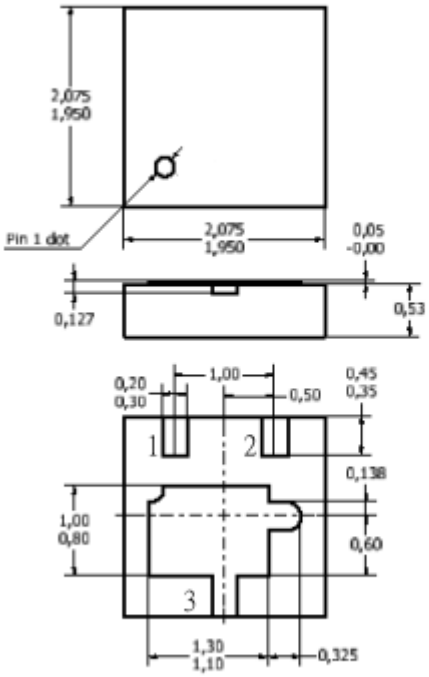


NOTES:

1. PINOUT (See Top View at left:)
   - Pin 1 NC
   - Pin 2 GND
   - Pin 3 NC
   - Pin 4 VDD
   - Pin 5 Out
2. Controlling dimension: mm;

QFN2x2-3L Package

(Top View)



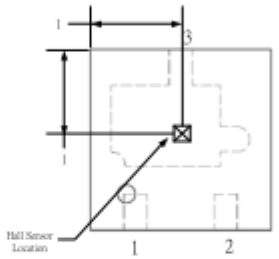
(Bottom View)

NOTES:

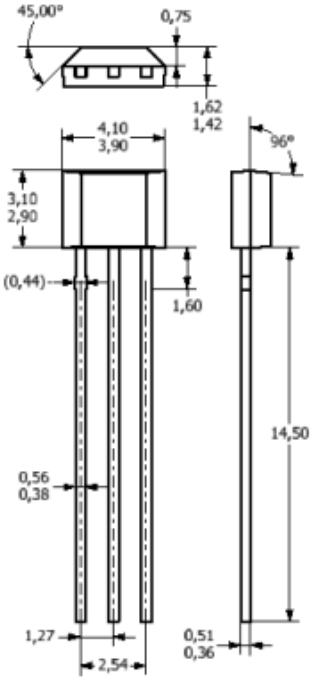
3. PINOUT (See Top View at left)
   Pin 1 VDD
   Pin 2 Output
   Pin 3 GND
4. Controlling dimension: mm;
5. Chip rubbing will be 10mil maximum;
6. Chip must be in PKG. center.

Hall Plate Chip Location

(Top view)



TO92-3L Package



NOTES:

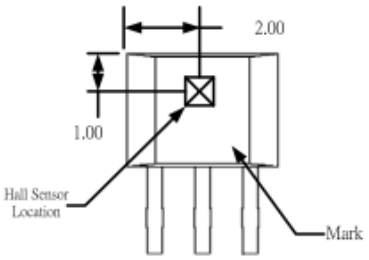
1).Controlling dimension: mm 2).Leads must be free of flash and plating voids

3).Do not bend leads within 1 mm of lead to package interface.

4).PINOUT:

Pin 1 VDD
Pin 2 GND
Pin 3 Output

Hall Chip location



Output Pin Assignment

(Top view)