

Three-wire Serial EEPROM

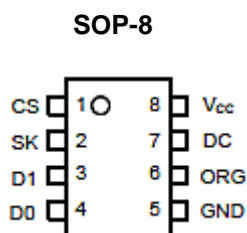
General Description

The EC93C56A/66A provides 2048/4096 bits of serial electrically erasable programmable read only memory (EEPROM) organized as 128/256 words of 16 bits each, when the ORG pin is connected to VCC and 256/512 words of 8 bits each when it is tied to ground. The EC93C56A/66A is available in space-saving PDIP-8, SOP-8, TSSOP-8, MSOP-8, and DFN-8 packages. The EC93C56A/66A is enabled through the Chip Select pin (CS), and accessed via a 3-wire serial interface consisting of Data Input (DI), Data Output (DO), and Shift Clock (SK). Upon receiving a Read instruction at DI, the address is decoded and the data is clocked out serially on the data output pin DO. The WRITE cycle is completely self-timed and no separate erase cycle is required before write. The Write cycle is only enabled when it is in the Erase/Write Enable state. When CS is brought "high" following the initiation of a write cycle, the DO pin outputs the Ready/Busy status.

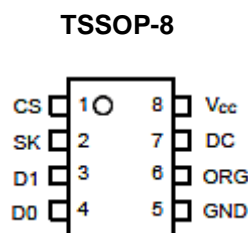
Features

- Low-voltage Operation
 - 1.7V (VCC = 1.7V to 5.5V)
- Three-wire Serial Interface
- Sequential Read Operation
- 2 MHz Clock Rate (5V) Compatibility
- Self-timed Write Cycle (5 ms max)
- High-reliability
 - Endurance: 1 Million Write Cycles
 - Data Retention: 100 Years
- PDIP-8, SOP-8, TSSOP-8, MSOP-8 and DFN-8 packages.

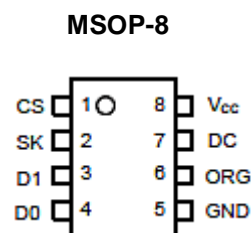
Pin Configuration



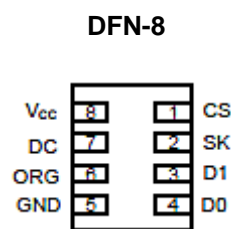
Top view



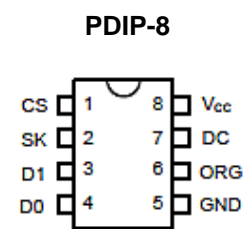
Top view



Top view



Bottom view

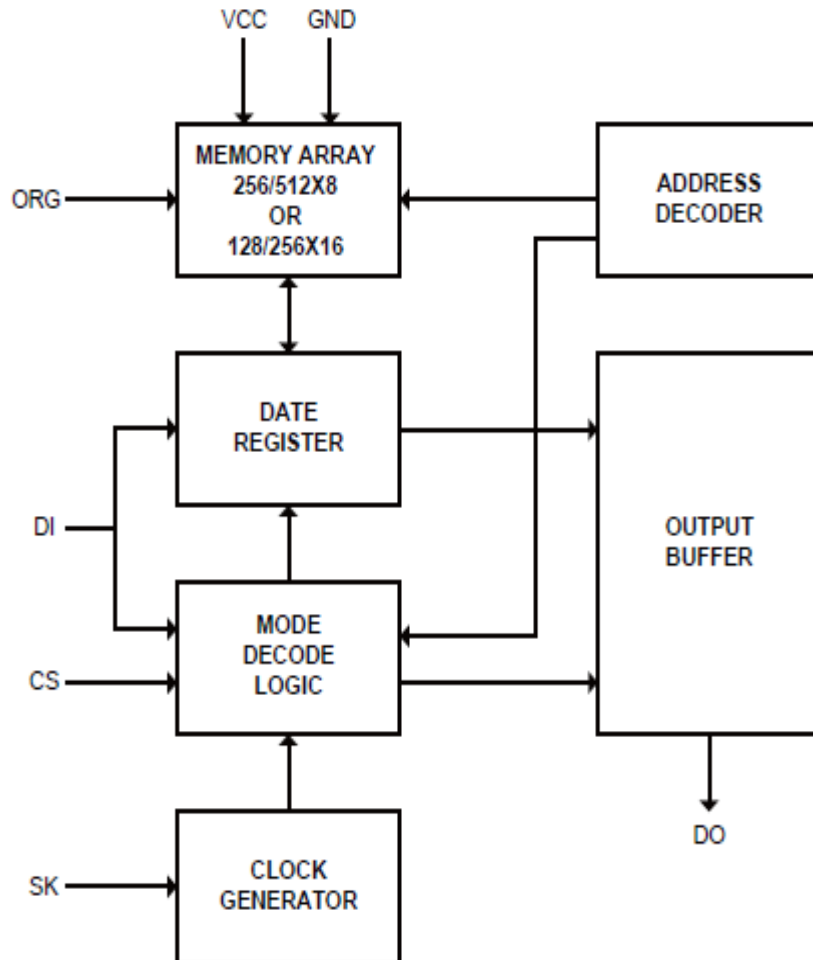


Top view

Pin Name	Functions
CS	Chip Select
SK	Serial Data Clock
DI	Serial Data Input
DO	Serial Data Output
GND	Ground
Vcc	Power Supply
ORG	Internal Organization
DC	Don't Connect

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Block Diagram



Notes: When the ORG pin is connected to VCC, the “x 16” organization is selected. When it is connected to ground, the “x 8” organization is selected. If the ORG pin is left unconnected and the application does not load the input beyond the capability of the internal 1 Meg ohm pullup, then the “x 16” organization is selected.

**Three-wire Serial EEPROM****Function Descriptions**

The EC93C56A/66A is accessed via a simple and versatile three-wire serial communication interface. Device operation is controlled by seven instructions issued by the host processor. A valid instruction starts with a rising edge of CS and consists of a start bit (logic“1”) followed by the appropriate op code and the desired memory address location.

Instruction set for the EC93C56A/66A

Instruction	SB	OP Code	Address		Data		Comments
			x8	x16	x8	x16	
READ	1	10	A ₈ - A ₀	A ₇ - A ₀			Reads data stored in memory, at specified address
EWEN	1	00	11XXXXXXXX	11XXXXXXXX			Write enable must precede all programming modes
ERASE	1	11	A ₈ - A ₀	A ₇ - A ₀			Erase memory location A _n - A ₀
WRITE	1	01	A ₈ - A ₀	A ₇ - A ₀	D ₇ - D ₀	D ₁₅ - D ₀	Writes memory location A _n - A ₀
ERAL	1	00	10XXXXXXXX	10XXXXXXXX			Erases all memory locations. Valid only at VCC=4.5V to 5.5V
WRAL	1	00	01XXXXXXXX	01XXXXXXXX	D ₇ - D ₀	D ₁₅ - D ₀	Writes all memory locations. Valid only at VCC=4.5V to 5.5V
EWDS	1	00	00XXXXXXXX	00XXXXXXXX			Disables all programming instructions

Notes: The X's in the address field represent don't care values and must be clocked.

READ (READ): The Read (READ) instruction contains the address code for the memory location to be read. After the instruction and address are decoded, data from the selected memory location is available at the serial output pin DO. Output data changes are synchronized with the rising edges of serial clock SK. It should be noted that a dummy bit (logic “0”) precedes the 8- or 16-bit data output string. The EC93C56A/66A supports sequential read operations. The device will automatically increment the internal address pointer and clock out the next memory location as long as Chip Select (CS) is held high. In this case, the dummy bit (logic “0”) will not be clocked out between memory locations, thus allowing for a continuous stream of data to be read.

ERASE/WRITE (EWEN): To assure data integrity, the part automatically goes into the Erase/Write Disable (EWDS) state when power is first applied. An Erase/Write Enable (EWEN) instruction must be executed first before any programming instructions can be carried out. Please note that once in the EWEN state, programming remains enabled until an EWDS instruction is executed or VCC power is removed from the part.

ERASE (ERASE): The Erase (ERASE) instruction programs all bits in the specified memory location to the logical “1” state. The self-timed erase cycle starts once the ERASE instruction and address are decoded. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (TCS). A logic “1” at pin DO indicates that the selected memory location has been erased, and the part is ready for another instruction.

WRITE (WRITE): The Write (WRITE) instruction contains the 8 or 16 bits of data to be written into the specified memory location. The self-timed programming cycle, tWP, starts after the last bit of data is received at serial data input pin DI. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (TCS). A logic “0” at DO indicates that programming is still in progress. A logic “1” indicates that the memory location at the specified address has been written with the data pattern contained in the instruction and the part is ready for further instructions. A Ready/Busy status cannot be obtained if the CS is brought high after the end of the self-timed programming cycle, TWP.

ERASE ALL (ERAL): The Erase All (ERAL) instruction programs every bit in the memory array to the logic “1” state and is primarily used for testing purposes. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (TCS). The ERAL instruction is valid only at VCC = 5.0V ± 10%.



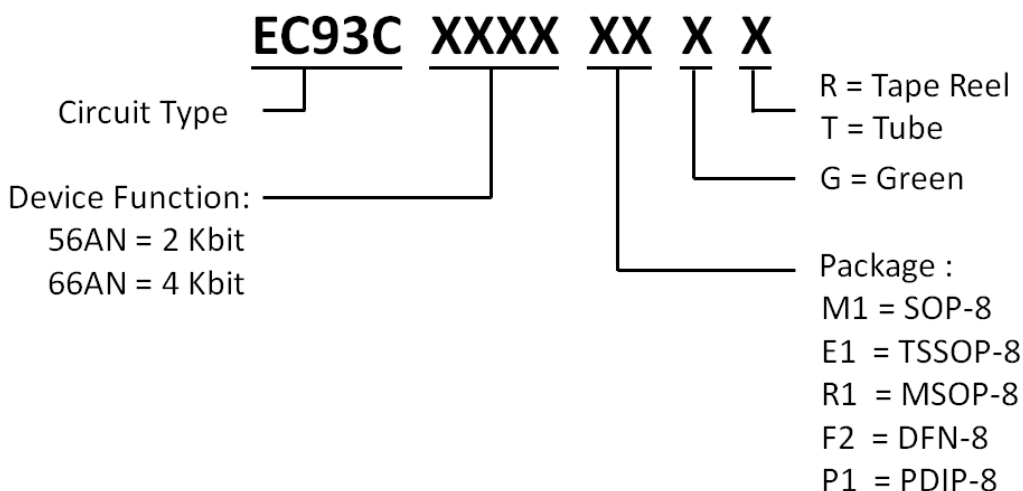
Three-wire Serial EEPROM

Function Descriptions

WRITE ALL (WRAL): The Write All (WRAL) instruction programs all memory locations with the data patterns specified in the instruction. The DO pin outputs the Ready/Busy status of the part if CS is brought high after being kept low for a minimum of 250 ns (TCS). The WRAL instruction is valid only at VCC = 5.0V ± 10%.

ERASE/WRITE DISABLE (EWDS): To protect against accidental data disturb, the Erase/Write Disable (EWDS) instruction disables all programming modes and should be executed after all programming operations. The operation of the Read instruction is independent of both the EWEN and EWDS instructions and can be executed at any time.

Ordering Information



Marking Information

Package Type	Part Number	Marking	Marking Information
SOP-8	EC93CXXANM1GX	93CXXA LLLLL YYWWT	LLLLL is the last five numbers of wafer lot number YYWW is Date Code. T is tracking Code ,T=X
TSSOP-8	EC93CXXANE1GX		
MSOP-8	EC93CXXANR1GX		
PDIP-8	EC93CXXANP1GX		
DFN-8	EC93CXXANF2GX	CXXA LLLL	XX is the memory of production. LLLL is the last four numbers of wafer lot number

Available Package Types

Part Number	SOP-8	TSSOP-8	MSOP-8	DFN-8	PDIP-8
EC93C56A	√	√	√	√	√
EC93C66A	√	√	√	√	√



Three-wire Serial EEPROM

Electrical Characteristics

Absolute Maximum Ratings

DC Supply Voltage -----	-0.3V to +6.5V
Input / Output Voltage -----	GND-0.3V to V _{CC} +0.3V
Operating Ambient Temperature -----	-40°C to +85°C
Storage Temperature -----	-65°C to +150°C

Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Characteristics

Applicable over recommended operating range from: T_A = -40°C to +85°C, V_{CC} = + 1.7V to + 5.5V (unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Units	
V _{CC1}	Supply Voltage	-	1.8	-	5.5	V	
V _{CC2}	Supply Voltage	-	2.7	-	5.5	V	
V _{CC3}	Supply Voltage	-	4.5	-	5.5	V	
I _{CC}	Supply Current	V _{CC} =5.0V	Read at 1.0 MHz	-	0.5	2.0	mA
			Write at 1.0 MHz	-	2	3.0	mA
I _{SB1}	Standby Current	V _{CC} =1.7V	-	-	1.0	μA	
I _{SB2}	Standby Current	V _{CC} =2.7V	-	-	1.0	μA	
I _{SB3}	Standby Current	V _{CC} =5.0V	-	-	1.0	μA	
I _{IL(1)}	Input Leakage	V _{IN} =0V to V _{CC}	-	0.1	1.0	μA	
I _{IL(2)}	Input Leakage	V _{IN} =0V to V _{CC}	-	2.0	3.0	μA	
I _{OL}	Output Leakage	V _{IN} =0V to V _{CC}	-	0.1	1.0	μA	
V _{IL1(3)}	Input Low Voltage	2.7V ≤ V _{CC} ≤ 5.5V	-0.3	-	0.8	V	
V _{IH1(3)}	Input High Voltage		2.0	-	V _{CC} +0.3	V	
V _{IL2(3)}	Input Low Voltage	1.8V ≤ V _{CC} ≤ 2.7V	-0.5	-	V _{CC} ×0.3	V	
V _{IH2(3)}	Input High Voltage		V _{CC} ×0.7	-	V _{CC} +0.3	V	
V _{IL3(3)}	Input Low Voltage	V _{CC} = 1.7V	-0.5	-	V _{CC} ×0.2	V	
V _{IH3(3)}	Input High Voltage		V _{CC} ×0.7	-	V _{CC} +0.3	V	
V _{OL1}	Output Low Voltage	2.7V ≤ V _{CC} ≤ 5.5V	-	-	0.4	V	
V _{OH1}	Output High Voltage		I _{OL} =2.1mA	2.4	-	-	V
V _{OL2}	Output Low Voltage	1.7V ≤ V _{CC} ≤ 2.7V	-	-	0.2	V	
V _{OH2}	Output High Voltage		I _{OH} =-100μA	V _{CC} -0.2	-	-	V

Notes:

- DI、CS、SK input pin
- ORG input pin
- V_{IL} min and V_{IH} max are reference only and are not tested.

Pin Capacitance

Applicable over recommended operating range from T_A = 25°C, f = 1.0 MHz, V_{CC} = +1.7V (unless otherwise noted)

Symbol	Test Conditions	Max	Unit	Conditions
CO _{UT}	Output Capacitance (DO)	5	pF	V _{OUT} = 0V
CIN	Input Capacitance (CS, SK, DI, ORG)	5	pF	V _{IN} = 0V



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AC Characteristics

Applicable over recommended operating range from $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{CC} = +1.7\text{V}$ to $+5.5\text{V}$
 $C_L = 1$ TTL Gate and 100pF (unless otherwise noted)

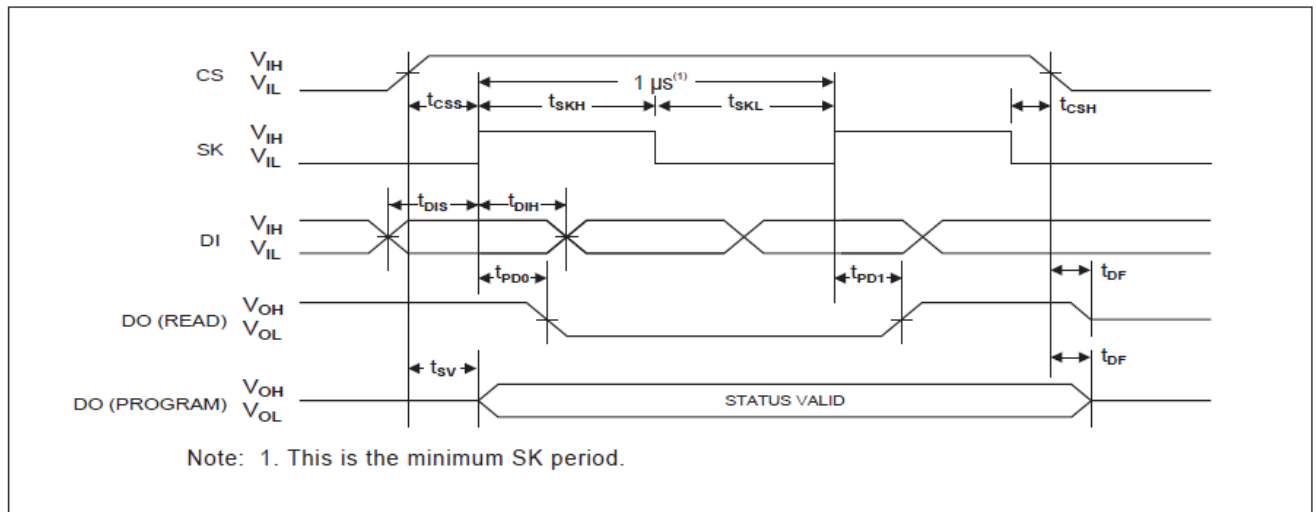
Symbol	Parameter	Test Condition	Min	Typ	Max	Units
f _{SK}	SK Clock Frequency	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	0	-	2	MHz
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	0		1	
		$1.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	0		0.25	
t _{SKH}	SK High Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	250	-	-	ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	250			
		$1.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	1000			
t _{SKL}	SK Low Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	250	-	-	ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	250			
		$1.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	1000			
t _{CS}	Minimum CS Low Time	$4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	250	-	-	ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	250			
		$1.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	1000			
t _{CSs}	CS Setup Time	Relative to SK $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	50	-	-	ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	50			
		$1.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	200			
t _{DIS}	DI Setup Time	Relative to SK $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	100	-	-	ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	100			
		$1.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	400			
t _{CSH}	CS Hold Time	Relative to SK	0	-	-	ns
t _{DIH}	DI Hold Time	Relative to SK $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	100	-	-	ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	100			
		$1.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	400			
t _{PD1}	Output Delay to "1"	AC Test $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	-	-	250	ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	-		250	
		$1.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	-		1000	
t _{PD0}	Output Delay to "0"	AC Test $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	-	-	250	ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	-		250	
		$1.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	-		1000	
t _{SV}	CS to Status Valid	AC Test $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	-	-	250	ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	-		250	
		$1.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	-		1000	
t _{DF}	CS to DO in High Impedance	AC Test CS = VIL $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$	-	-	100	ns
		$2.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	-		100	
		$1.7\text{V} \leq V_{CC} \leq 5.5\text{V}$	-		400	
t _{WP}	Write Cycle Time	-	-	1.5	5	ms
Endurance ⁽¹⁾	5.0V, 25°C	-	1M	-	-	Write Cycle

Note: 1. This parameter is characterized and is not 100% tested.

Three-wire Serial EEPROM

Timing Diagrams

Synchronous Data Timing



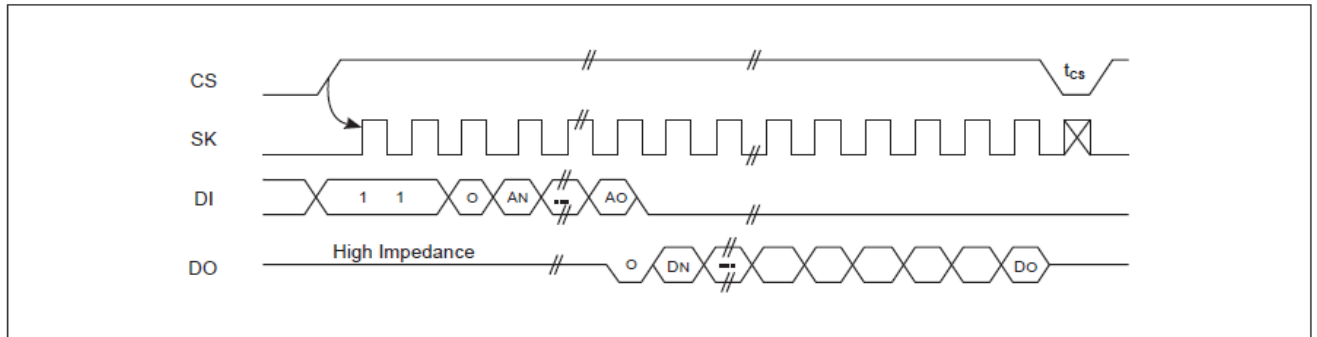
Organization Key for Timing Diagram

I/O	EC93C56A(2K)		EC93C66A(4K)	
	X 8	X 16	X 8	X 16
AN	A8(1)	A7(2)	A8	A7
DN	D7	D15	D7	D15

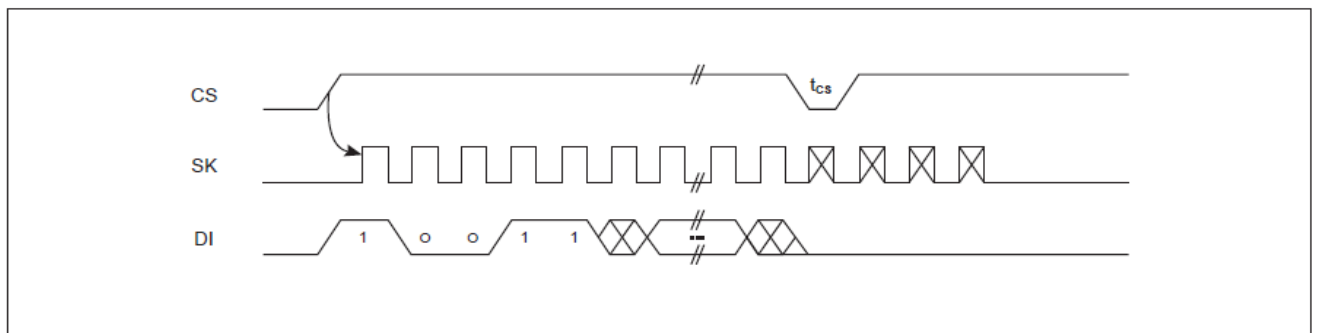
Note : 1. A8 is a DON'T CARE value, but the extra clock is required.
 2. A7 is a DON'T CARE value, but the extra clock is required.

Three-wire Serial EEPROM

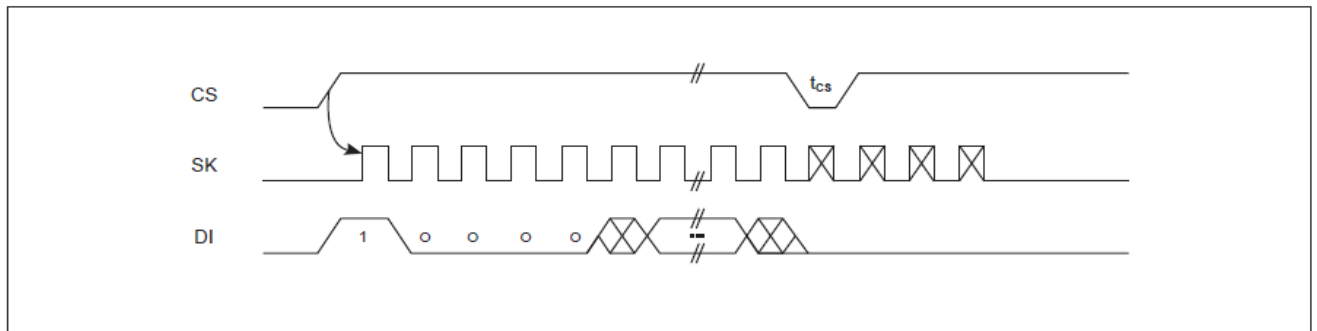
READ Timing



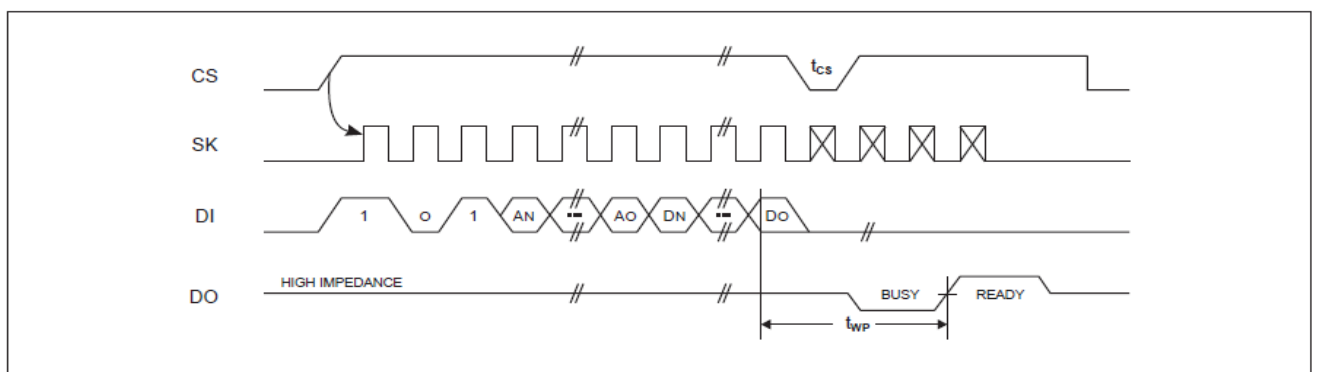
EWEN Timing



EWDS Timing

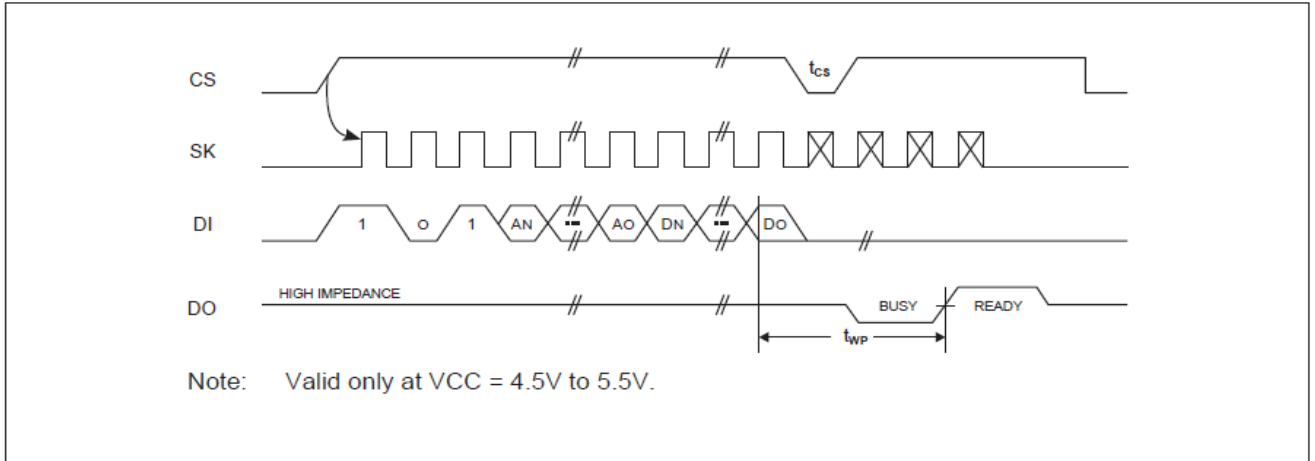


WRITE Timing

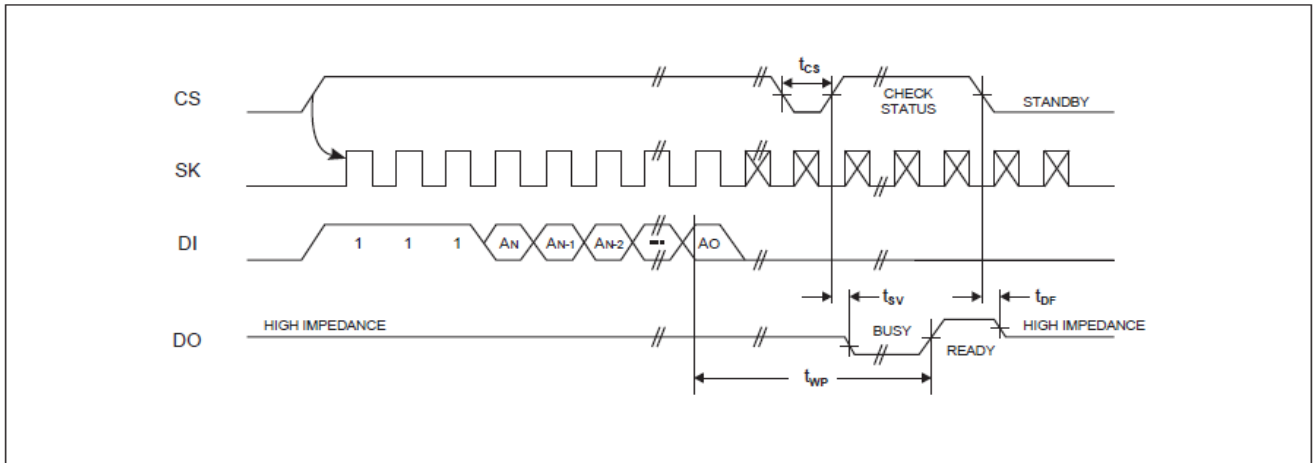


Three-wire Serial EEPROM

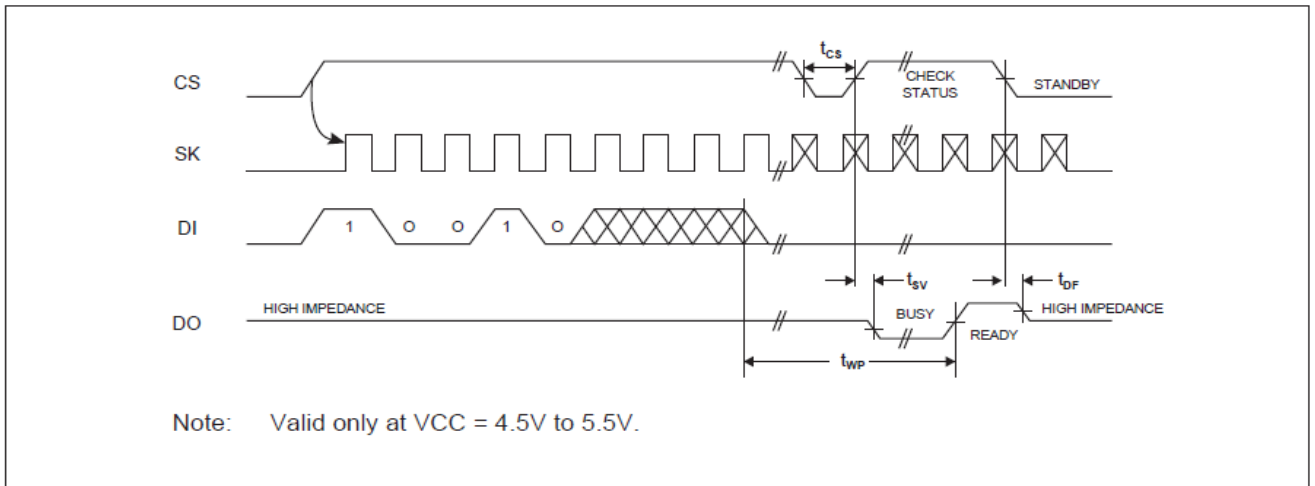
WRAL Timing



ERASE Timing



ERAL Timing



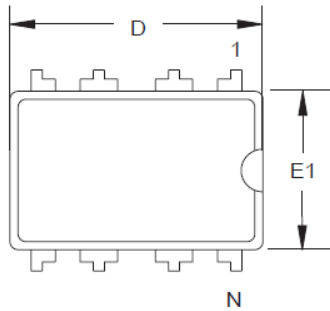
Three-wire Serial EEPROM

Mechanical Dimensions

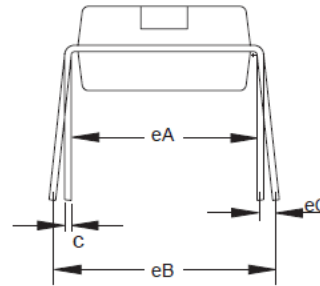
OUTLINE DRAWING PDIP - 8

Available package types : EC93C56A/66A

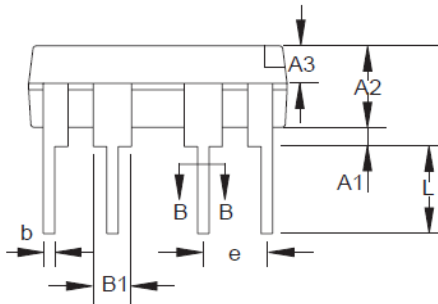
Top View



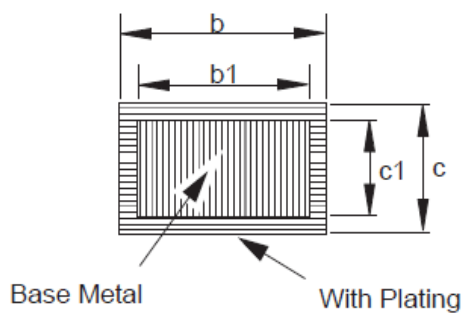
End View



Side View



Section B - B



COMMON DIMENSIONS (Unit of Measure = mm)

SYMBOL	MIN	MAX
A	3.60	4.00
A1	0.51	-
A2	3.10	3.50
A3	1.50	1.70
b	0.44	0.53
b1	0.43	0.48
B	1.52 BSC	
c	0.25	0.31
c1	0.24	0.26
D	9.05	9.45
E1	6.15	6.55
e	2.54 BSC	
eA	7.62 BSC	
eB	7.62	9.50
eC	0	0.94
L	3.00	-

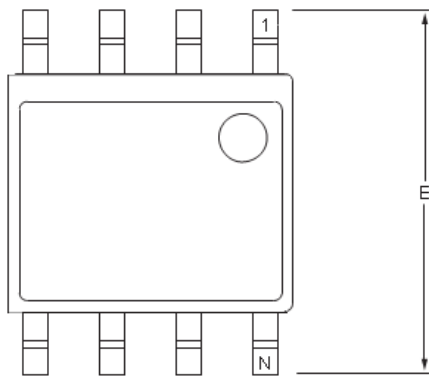
Three-wire Serial EEPROM

Mechanical Dimensions

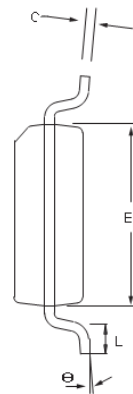
OUTLINE DRAWING SOP - 8

Available package types : EC93C56A/66A

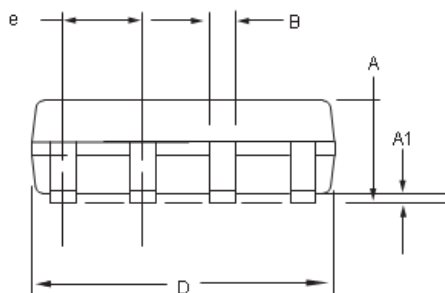
Top View



End View



Side View



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
b	0.31	0.51
C	0.17	0.25
D	4.70	5.10
E1	3.80	4.00
E	5.79	6.20
e	1.27 BSC	
L	0.40	1.27
θ	0°	8°

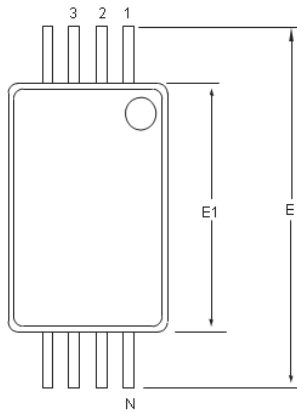
Three-wire Serial EEPROM

Mechanical Dimensions

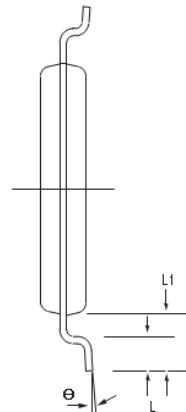
OUTLINE DRAWING TSSOP - 8

Available package types : EC93C56A/66A

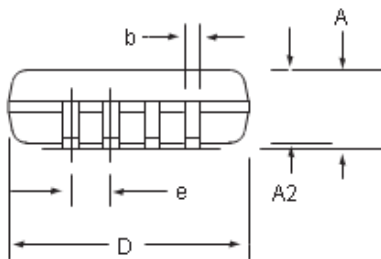
Top View



End View



Side View



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	MAX
D	2.80	3.20
E	6.20	6.60
E1	4.20	4.60
A	-	1.20
A2	0.80	1.15
b	0.19	0.30
e	0.65 BSC	
L	0.45	0.75
L1	1.00 BSC	
θ	0°	8°

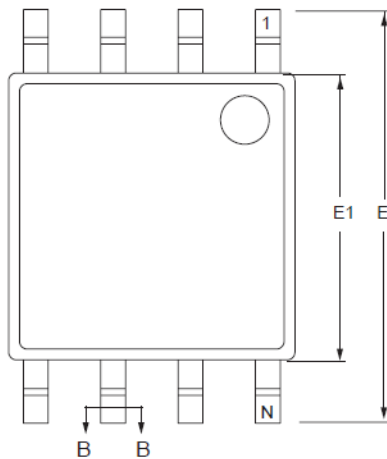
Three-wire Serial EEPROM

Mechanical Dimensions

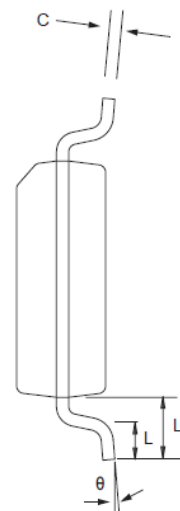
OUTLINE DRAWING MSOP - 8

Available package types : EC93C56A/66A

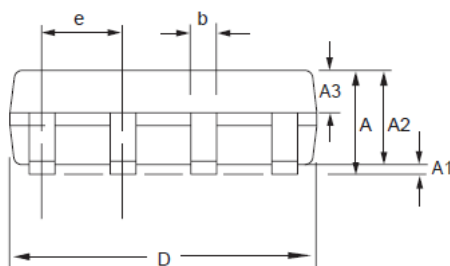
Top View



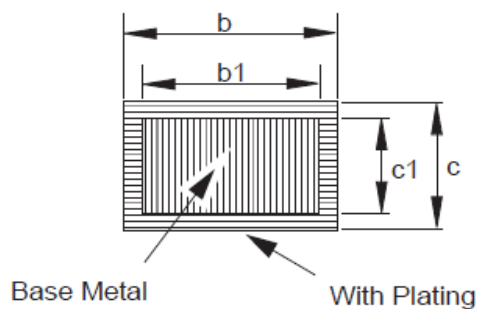
End View



Side View



Section B - B



COMMON DIMENSIONS (Unit of Measure = mm)

SYMBOL	MIN	MAX
A	-	1.10
A1	0.05	0.15
A2	0.75	0.95
A3	0.30	0.40
b	0.29	0.38
b1	0.28	0.33
c	0.15	0.20
c1	0.14	0.16
D	2.90	3.10
E	4.70	5.10
E1	2.90	3.10
e	0.65 BSC	
L	0.40	0.70
L1	0.95 BSC	
θ	0°	8°

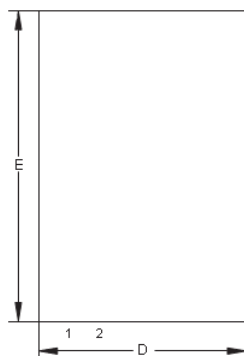
Three-wire Serial EEPROM

Mechanical Dimensions

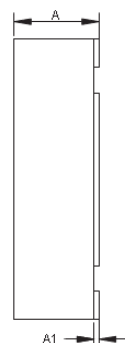
OUTLINE DRAWING DFN - 8

Available package types : EC93C56A/66A

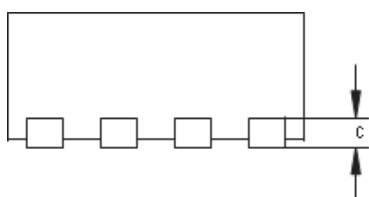
Top View



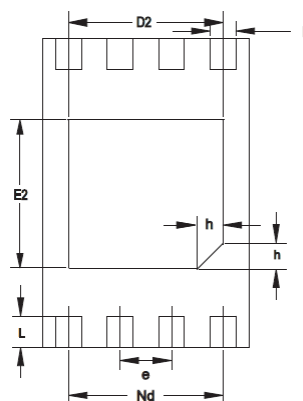
End View



Side View



Bottom View



COMMON DIMENSIONS

(Unit of Measure = mm)

SYMBOL	MIN	MAX
A	0.70	0.80
A1	-	0.05
b	0.18	0.30
c	0.18	0.25
D	1.90	2.10
D2	1.50 REF	
e	0.50 BSC	
Nd	1.50 BSC	
E	2.90	3.10
E2	1.60 BSC	
L	0.30	0.50
h	0.20	0.30