Description

The EJW5057C is a current mode monolithic buck voltage converter. Operating with an input range of 4.5V-17V, the EJW5057C delivers 3A of continuous output current with two integrated N-Channel MOSFETs. At light loads, regulators operate in low frequency to maintain high efficiency and low output ripple. The EJW5057C guarantees robustness with short circuit protection, thermal protection, current run-away protection, and input under voltage lockout. The EJW5057C is available in a 6-pin SOT23-6 package, which provides a compact solution with minimal external components.

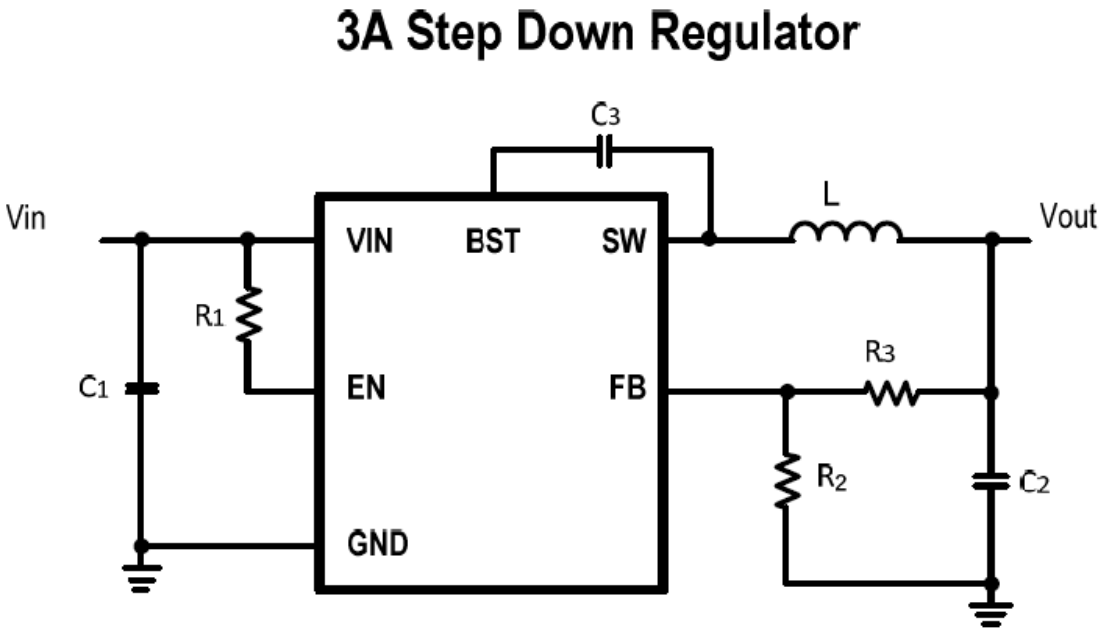
Features

◆4.5V to 17V operating input range 3A output current
◆Up to 93% efficiency
◆High efficiency at light load
◆Fixed 500kHz Switching frequency
◆Input under voltage lockout
◆Start-up current run-away protection
◆Over current protection and Hiccup
◆Thermal protection
◆Available in SOT23-6 package

Applications

◆Distributed Power Systems
◆Networking Systems
◆FPGA, DSP, ASIC Power Supplies
◆Green Electronics/ Appliances
◆Notebook Computers

Typical application



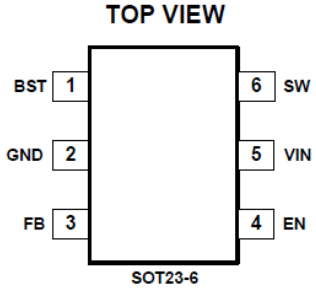
Ordering/Marking Information

EJW5057C XX X X

- XX: Package Type：B3：SOT23-6
- X: F：Pb Free, G：Green
- X: R：Tape & Reel

Device	Marking	Package	Information
EJW5057CB3XR	JWK7X YWLLL	SOT23-6	K7：Product code X：Internal control Code Y：Year Code W：Week Code LLL：Lot number

Pin Configurations



Absolute Maximum Ratings[1)]

VIN, EN Pin >..... -0.3V to 20V
SW..... -0.3V(-4.5V for 10ns) to 20V(22V for 10ns)
BST Pin ..... SW-0.3V to SW+5V
All other Pins ..... -0.3V to 6V
Junction Temp. 2) 3) 150ºC
Lead Temperature 260ºC
ESD Susceptibility (Human Body Model) 2kV

Recommended Operating Conditions

Input Voltage VIN ..... 4.5V to 17V
Output Voltage Vout .....0.6V to VIN-3V

Thermal Performance[4)]

	θ_{JA}	θ_{JC}
SOT23-6	220	130ºC/W

Note：
1) Exceeding these ratings may damage the device.
2) The EJW5057C guarantees robust performance from -40°C to 150°C junction temperature. The junction temperature range specification is assured by design, characterization and correlation with statistical process controls.
3) The EJW5057C includes thermal protection that is intended to protect the device in overload conditions. Thermal protection is active when junction temperature exceeds the maximum operating junction temperature. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
4) Measured on JESD51-7, 4-layer PCB

Electrical Characteristics VIN=12V, TA=25℃Unless otherwise stated

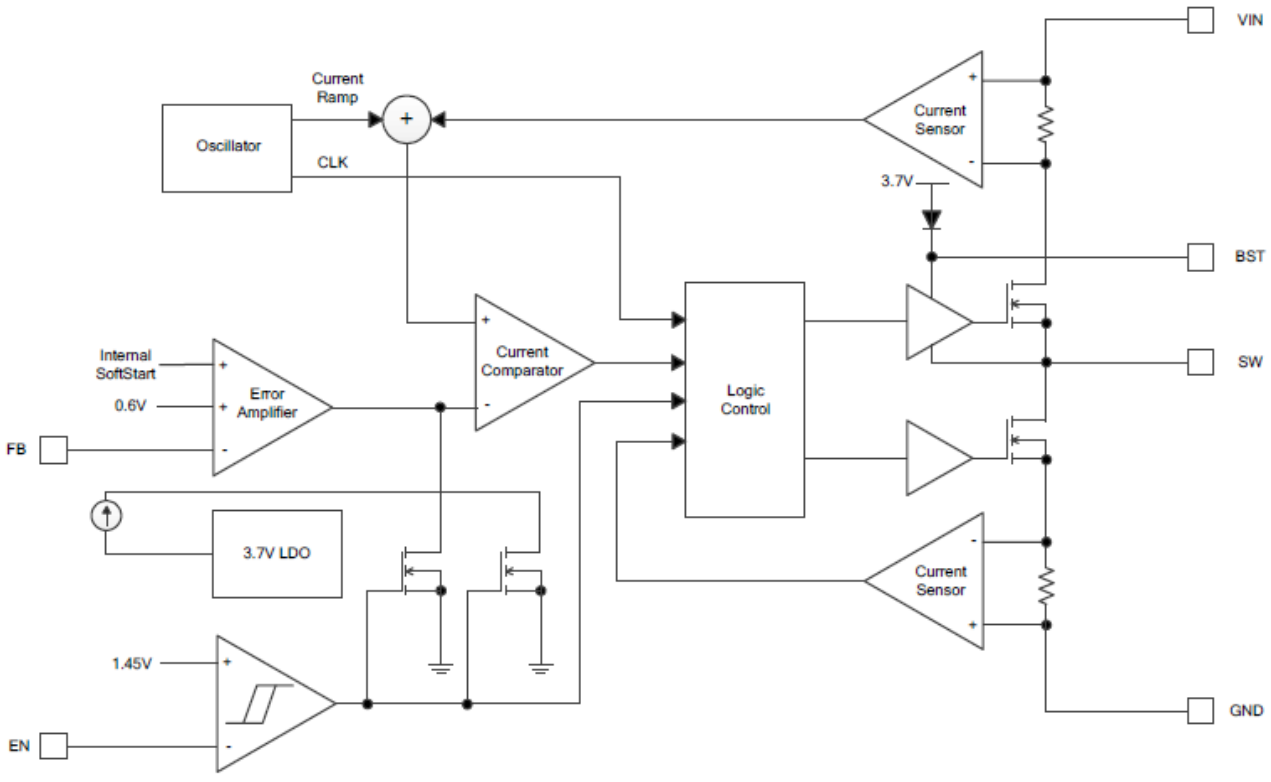
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
VIN Under Voltage Lock-out Threshold	V_{IN_MIN}	V_{IN} rising		4.2	4.45	V
VIN Under voltage Lockout Hysteresis5)	$V_{IN\_MIN\_HYST}$			300		mV
Shutdown Supply Current	I_{SD}	V_{EN}=0V		0.1	1	μA
Supply Current	I_Q	V_{EN}=5V, V_{FB}=1.2V		100	130	μA
Feedback Voltage	V_{FB}	4.5V<V_{VIN}<17V	588	600	612	mV
Top Switch Resistance5)	$R_{DS(ON)T}$			90		m
Bottom Switch Resistance5)	$R_{DS(ON)B}$			50		m
Top Switch Leakage Current	I_{LEAK_TOP}	V_{IN}=17V, V_{EN}=0V, V_{SW}=0V		0.1	1	μA
Bottom Switch Leakage Current	I_{LEAK_BOT}	V_{IN}=17V, V_{EN}=0V, V_{SW}=17V		0.1	1	μA
Top Switch Current Limit5)	I_{LIM_TOP}	Minimum Duty Cycle	3.6	4.5	5.4	A
Switch Frequency	F_{SW}		375	500	625	kHz
Minimum On Time5)	T_{ON_MIN}			120		ns
Minimum Off Time5)	T_{OFF_MIN}	V_{FB}=0.4V		150		ns
EN high level input voltage	V_{EN_H}	V_{EN} rising	1.5			V
EN low level input voltage	V_{EN_L}	V_{EN} falling			1	V
Soft-Start Time5)	t_{SS}			1		ms
Thermal Shutdown5)	T_{TSD}			165		°C
Thermal Shutdown hysteresis5)	T_{TSD_HYST}			20		°C

Note：
5) Guaranteed by design.

Pin Description

Pin	Name	Description
1	BST	Bootstrap pin for top switch. A 0.1uF or larger capacitor should be connected between this pin and the SW pin to supply current to the top switch and top switch driver.
2	GND	Ground.
3	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 0.6V. Connect a resistive divider at FB.
4	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator.
5	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 4.5V to 17V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
6	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.

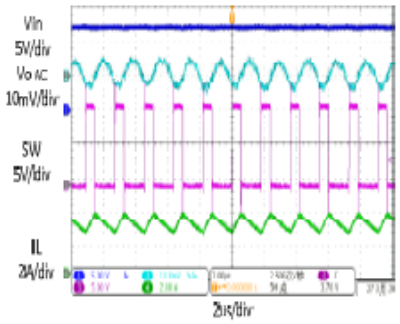
Block Diagram



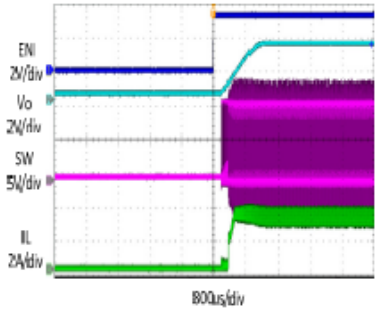
Typical Performance Characteristics

Vin =12V, Vout = 3.3V, L = 4.7μH, Cout = 22μF，TA = +25°C, unless otherwise noted

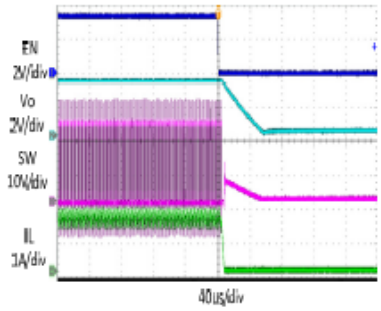
Steady State Test
VIN=12V, Vout=3.3V
Iout=3A



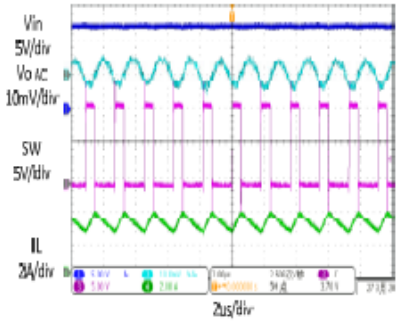
Startup through Enable
VIN=12V, Vout=3.3V
Iout=3A(Resistive load)



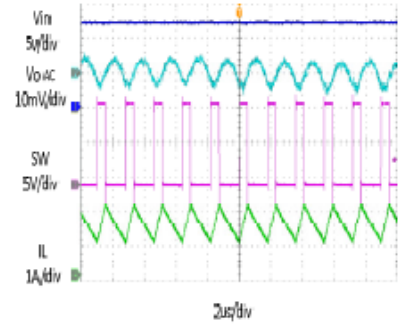
Shutdown through Enable
VIN=12V, Vout=3.3V
Iout=3A (Resistive load)



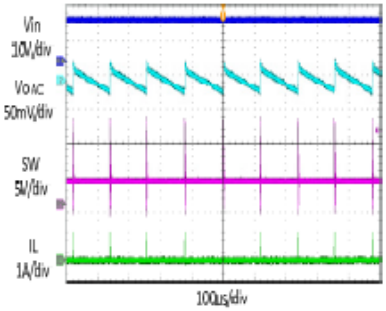
Heavy Load Operation
3A LOAD



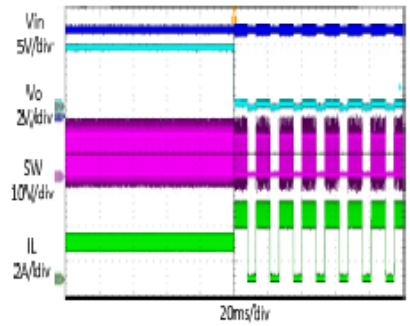
Medium Load Operation
1.5A LOAD



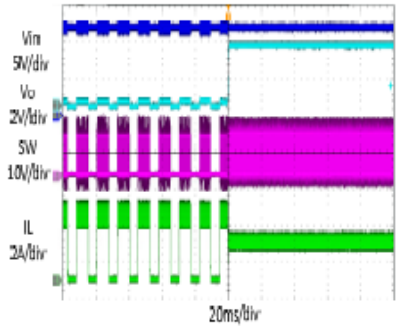
Light Load Operation
0A LOAD



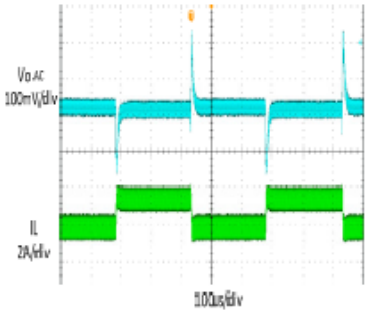
Short Circuit Protection
VIN=12V, Vout=3.3V
Iout=3A- Short



Short Circuit Recovery
VIN=12V, Vout=3.3V
Iout= Short-3A



Load Transient
1.5A LOAD →3A LOAD → 1.5A LOAD



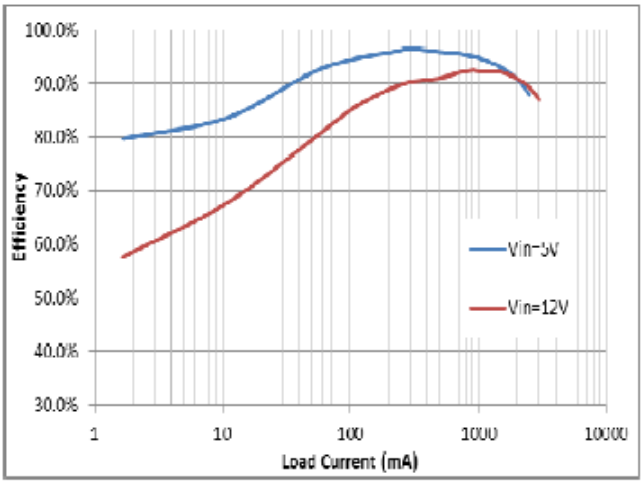


Figure 1. Efficiency vs Load Current

(Vout=3.3V, L=4.7uH)

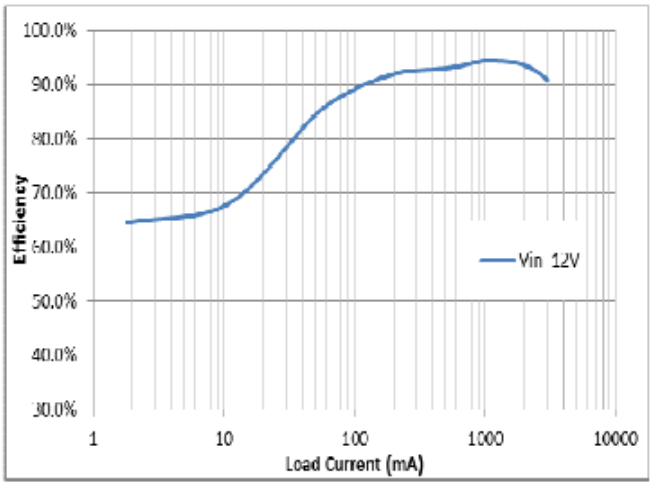


Figure 1. Efficiency vs Load Current

(Vout=5V, L=4.7uH)

Functional Description

The EJW5057C is a synchronous, current-mode, step-down regulator. It regulates input voltages from 4.5V to 17V down to an output voltage as low as 0.6V, and is capable of supplying up to 3A of load current.

Current-Mode Control

The EJW5057C utilizes current-mode control to regulate the FB voltage. Voltage at the FB pin is regulated at 0.6V so that by connecting an appropriate resistive divider between VOUT and GND, designed output voltage can be achieved.

PFM Mode

The EJW5057C operates in PFM mode at light load. In PFM mode, switch frequency decreases when load current drops to boost power efficiency at light load by reducing switch-loss, while switch frequency increases when load current rises, minimizing output voltage ripples.

Internal Soft-Start.

Soft-Start makes output voltage rising smoothly follow an internal SS voltage until SS voltage is higher than the internal reference voltage. It can prevent overshoot of output voltage when startup.

Power Switch

N-Channel MOSFET switches are integrated on the EJW5057C to down convert the input voltage to the regulated output voltage. Since the top MOSFET needs a gate voltage greater than the input voltage, a boost capacitor connected between BST and SW pins is required to drive the gate of the top switch. The boost capacitor is charged by the internal 3.7V rail when SW is low.

Vin Under-Voltage Protection

A resistive divider can be connected between Vin and GND, with the central tap connected to EN, so that when Vin drops to the pre-set value, EN drops below 1.2V to trigger input under voltage lockout protection.

Output Current Run-Away Protection

At start-up, due to the high voltage at input and low voltage at output, current inertia of the output inductance can be easily built up, resulting in a large start-up output current. A valley current limit is designed in the EJW5057C so that only when output current drops below the valley current limit can the top power switch be turned on. By such control mechanism, the output current at start-up is well controlled.

Over Current Protection and Hiccup

EJW5057C has a cycle-by-cycle current limit.

When the inductor current triggers current limit, EJW5057C enters hiccup mode and periodically restart the chip. EJW5057C exits hiccup mode while not triggering current limit.

Thermal Protection

When the temperature of the EJW5057C rises above 165°C, it is forced into thermal shut-down. Only when core temperature drops below 145°C can the regulator becomes active again.

Application Information

Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} \cdot \frac{R_2}{R_2 + R_3}$$

where VFB is the feedback voltage and VOUT is the output voltage.
Choose R2 around 10kM, and then R3 can be calculated by:

$$R_3 = R_2 \left(\frac{V_{OUT}}{0.6V} - 1 \right)$$

Too large resistance and the following table lists the recommended values.

VOUT(V)	R2(kΩ)	R3(kΩ)
1.2	10.2	10.2
3.3	11	49.9
5	15	110

Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. The ripple current through the input capacitor can be calculated by:

$$I_{C1} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)}$$

where ILOAD is the load current, VOUT is the output voltage, VIN is the input voltage.

Thus the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_1 = \frac{I_{LOAD}}{f_S \cdot \Delta V_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right)$$

where C1 is the input capacitance value, fs is the switching frequency, △VIN is the input ripple voltage.
The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1uF, should be placed as close to the IC as possible when using electrolytic capacitors. A 22~66uF ceramic capacitor is recommended in typical application.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \cdot \left(R_{ESR} + \frac{1}{8 \cdot f_S \cdot C_2} \right)$$

where C2 is the output capacitance value and RESR is the equivalent series resistance value of the output capacitor. The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage. The output capacitors also affect the system stability and transient response, and a 22~66Uf ceramic capacitor is recommended in typical application.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 40% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_S \cdot \Delta I_L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where VIN is the input voltage, VOUT is the output voltage, fs is the switching frequency, and △IL is the peak-to-peak inductor ripple current.

External Bootstrap Capacitor

A bootstrap capacitor is required to supply voltage to the top switch driver. A 0.1uF low ESR ceramic capacitor is recommended to connected to the BST pin and SW pin.

PCB Layout Note

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.
1. close to EJW5057C (VIN pin and PGND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as far away from the inductor and noisy power traces as possible.
3. The ground plane on the PCB should be as large as possible for better heat dissipation.

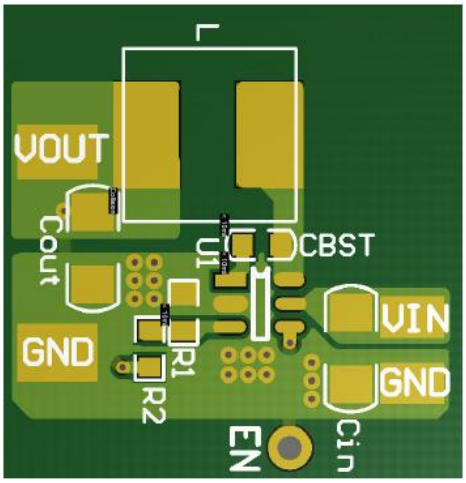
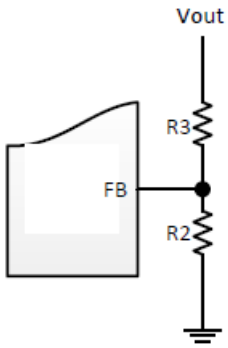


Figure1. PCB Layout Recommendation

External Components Suggestion

VOUT(V)	R2 (kΩ)	R3 (kΩ)	L(uH)	Cout(uF)
1	10.2	6.8	2.2~4.7	44~66
1.2	10.2	10.2	2.2~4.7	44~66
1.5	10	15	2.2~4.7	44~66
2.5	10	31.6	2.2~4.7	22~66
3.3	11	49.9	4.7	22~66
5	15	110	4.7	22~66

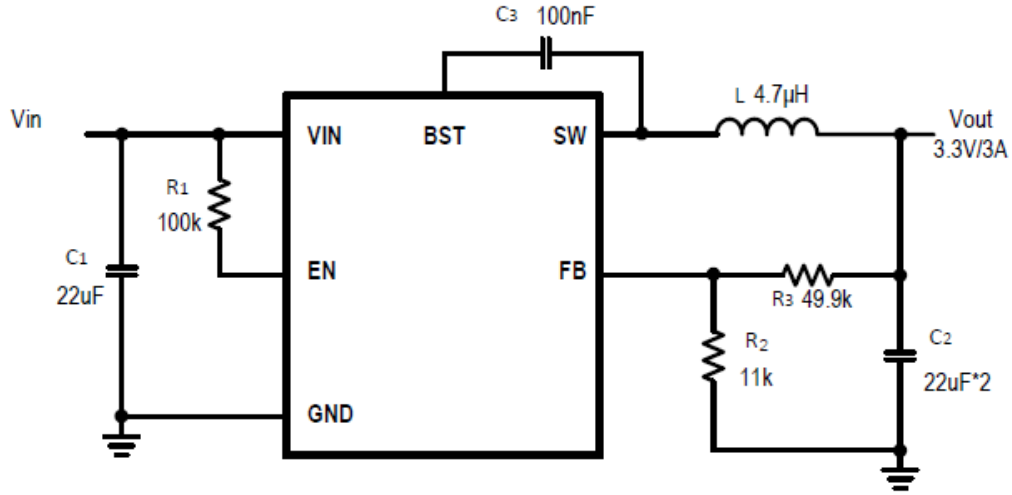


Reference Design

Reference 1

V_{OUT}: 3.3V

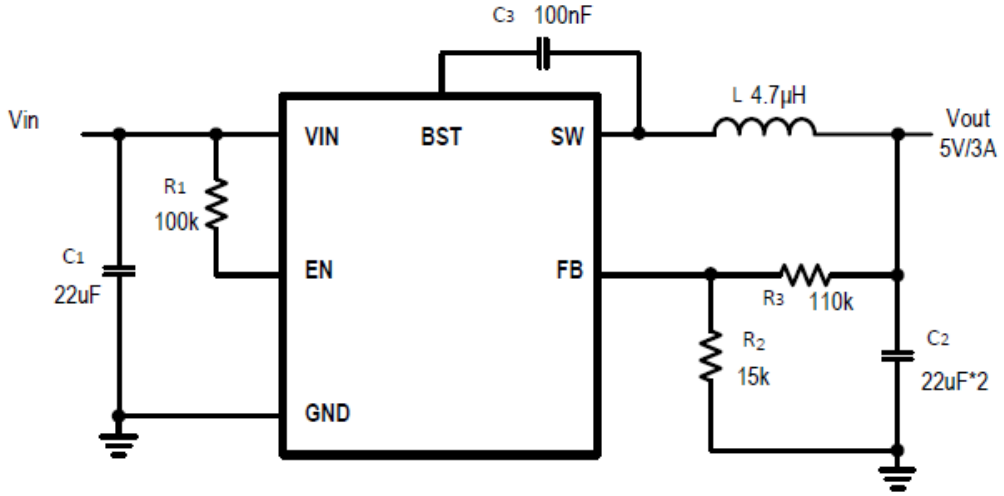
I_{OUT} : 0~3A



Reference 2

V_{OUT}: 5V

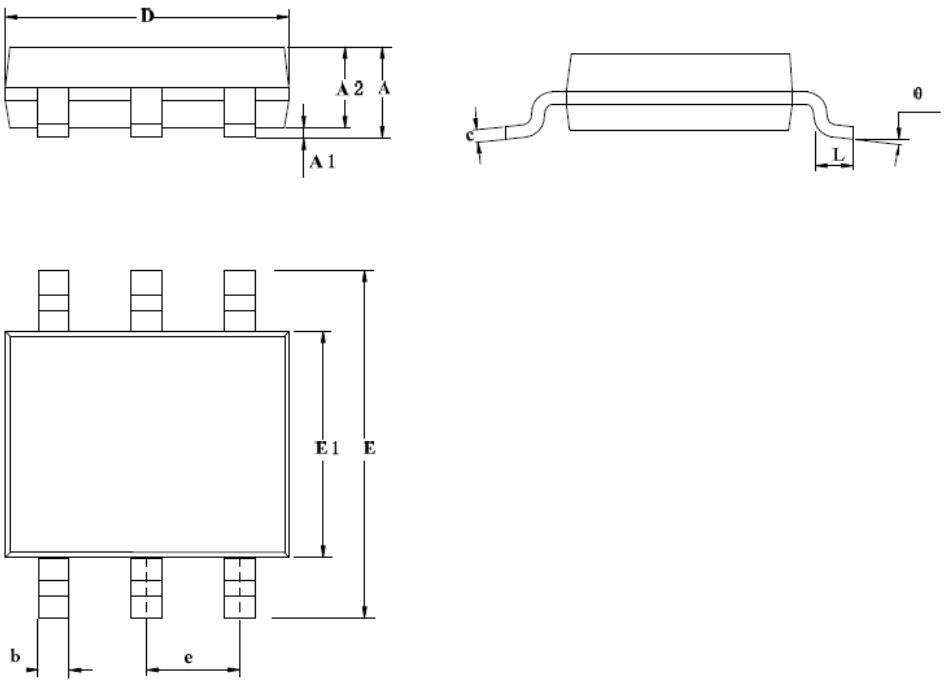
I_{OUT} : 0~3A



Package Outline

SOT23-6

UNIT: mm



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	1.05	1.15	1.25
A1	0	0.05	0.15
A2	0.95	1.05	1.20
b	0.20	0.40	0.60
c	0.05	—	0.21
D	2.72	2.92	3.12
E	2.60	2.80	3.00
E1	1.40	1.60	1.80
e	0.95 (BSC)		
L	0.30	0.45	0.60
θ	0°	—	8°