Description

The EJW5080 is a monolithic buck switching regulator based on constant-on time architecture for fast transient response. Operating with an input range of 3.3V~18V, EJW5080 delivers 8A of continuous output current with two integrated N-Channel MOSFETs. The internal synchronous power switches provide high efficiency without the use of an external Schottky diode. At light loads, the regulator operates in low frequency to maintain high efficiency and low output ripples. EJW5080 guarantees robustness with output short protection, thermal protection, current run-away protection, input under voltage lockout, hot-plug in protection, and FB short protection. EJW5080 is available in QFN3*4 package, which provides a compact solution with minimal external components.

Features

◆3.3V to 18V operating input range
◆8A output current
◆High efficiency (>85%) at light load
◆Programmable switching frequency
◆Tracked soft-start
◆Input under voltage lockout
◆Hot-plug in protection
◆Feedback short protection
◆Current run-away protection
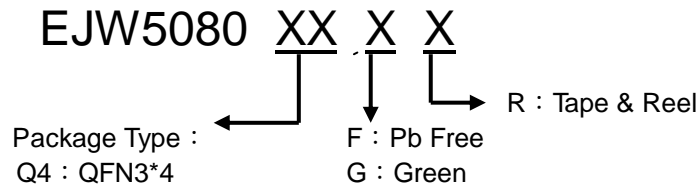◆Output short protection
◆Thermal protection
◆Available in QFN3*4 package

Applications

◆Distributed Power Systems
◆Networking Systems
◆FPGA, DSP, ASIC Power Supplies
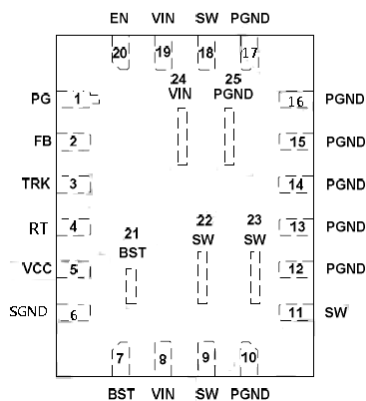◆Green Electronics/ Appliances
◆Notebook Computers

Typical Application

18V/8A Step Down Regulator
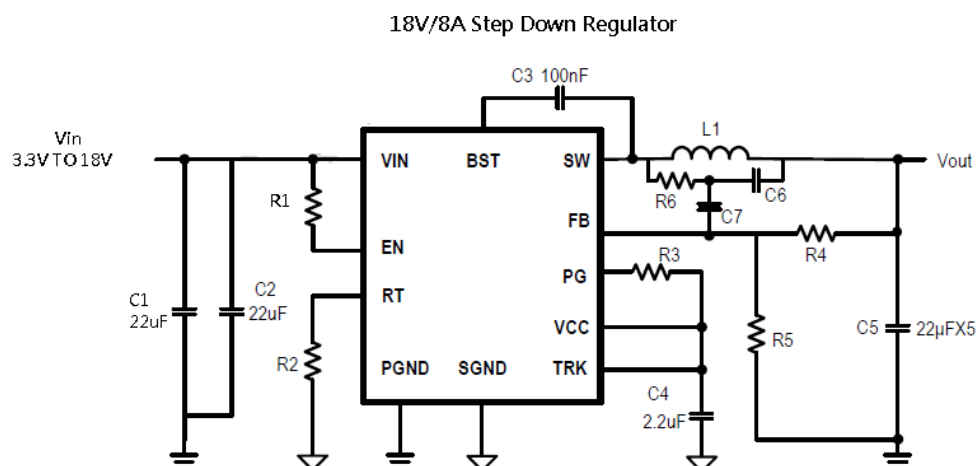
Ordering/Marking Information

EJW5080 XX X X

Package Type：
Q4：QFN3*4

F：Pb Free
G：Green

R：Tape & Reel

Device	Marking	Package	Information
EJW5080Q4XR	JW5080 XXXXXX	QFN3*4	XXXXXX: Date Code.

Pin Configurations

TOP VIEW

Absolute Maximum rating[1)]

VIN, EN, SW, FB, PG, TRK, RT Pin... -0.3V to 20V
BST Pin... SW-0.3Vto SW+5V
All other Pins .... -0.3V to 6V
Junction Temp. 2) 3) 150ºC
Lead Temperature 260ºC

Recommended Operating Conditions

Input Voltage VIN .... 3.3V to 18V
Output Voltage Vout 0.6Vto VIN-3V

Thermal Performance[4)]

θ_{JA} θ_{JC}

QFN3×4.. 46......9ºC/W

Note

1) Exceeding these ratings may damage the device.
2) The EJW5080 guarantees robust performance from -40°C to 150°C junction temperature. The junction temperature range specification is assured by design, characterization and correlation with statistical process controls.
3) The EJW5080 includes thermal protection that is intended to protect the device in overload conditions. Thermal protection is active when junction temperature exceeds the maximum operating junction temperature. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
4) Measured on JESD51-7, 4-layer PCB.

Electrical Characteristics

VIN=12V, TA=25 Unless otherwise stated							
Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
VIN Under Voltage Lock-out Threshold	VIN_MIN	VIN rising		2.8		V
VIN Under voltage Lockout Hysteresis	VIN_MIN_HYST			200		mV
Hot-plug In Protection Voltage Threshold	VOVP	VIN rising		21.6		V
Hot-plug In Protection Voltage Hysteresis	VOVP _HYST			3.6		V
Shutdown Supply Current	ISD	VEN=0V			1	µA
Supply Current	IQ	VEN=5V, VFB=1.2V		800		µA
Feedback Voltage	VFB	4.7V<VVIN<18V	591	600	609	mV
Top Switch Resistance[5]	RDS(ON)T			18		m
Bottom Switch Resistance[5]	RDS(ON)B			10		m
Top Switch Leakage Current	ILEAK_TOP	VIN=18V, VEN=0V, VSW=0V			1	µA
Bottom Switch Leakage Current	ILEAK_BOT	VIN=18, VEN=0V, VSW=0V			1	µA
Top Switch Current Limit	ILIM_TOP	Minimum Duty Cycle	11	14	17	A
Bottom Switch Current Limit	ILIM_BOT		8	10	12	A
Minimum On Time	TON_MIN			60		ns
Minimum Off Time	TOFF_MIN	VFB=0.4V		170		ns
EN shut down threshold voltage	VEN_TH	VEN rising	1.08	1.1	1.12	V
EN shut down hysteresis	VEN_HYST		95	100	105	mV
Soft-Start Period	TSS			0.8		ms
Power good lower threshold	PGD_LTH	FB falling		84%		
Power good upper threshold	PGD_UTH	FB rising		116%		
Power good delay	PGD_DLY	PG from low to high		1		ms
Thermal Shutdown[5]	TTSD			140		°C
Thermal Shutdown hysteresis[5]	TTSD_HYST			15		°C

Note

5) Guaranteed by design.

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Pin Description

Pin	Name	Description
1	PG	Power good monitor output. This is an open-drain output so a resistor should be connected at this pin to the VCC pin.
2	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 0.6V. Connect a resistive divider at FB.
3	TRK	For tracking start-up to other regulator, connect this pin to an external ramp. For internal soft-start, connect this pin to the VCC pin.
4	RT	Connect a resistor at RT to GND to program the on-time of the top switch.
5	VCC	Output of the internal LDO. Connect a 2.2uF capacitor at this pin.
6	SGND	Signal ground pin.
7, 21	BST	Connect a 0.1uF capacitor between BST and SW pin to supply current for the top switch driver.
8,19,24	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 3.3V to 18V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
9,11,18,22,23	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
10,12,13,14, 15,16,17,25	PGND	Power ground pin.
20	EN	Drive EN pin high to turn on the regulator and low to turn off the regulator.

Block Diagram

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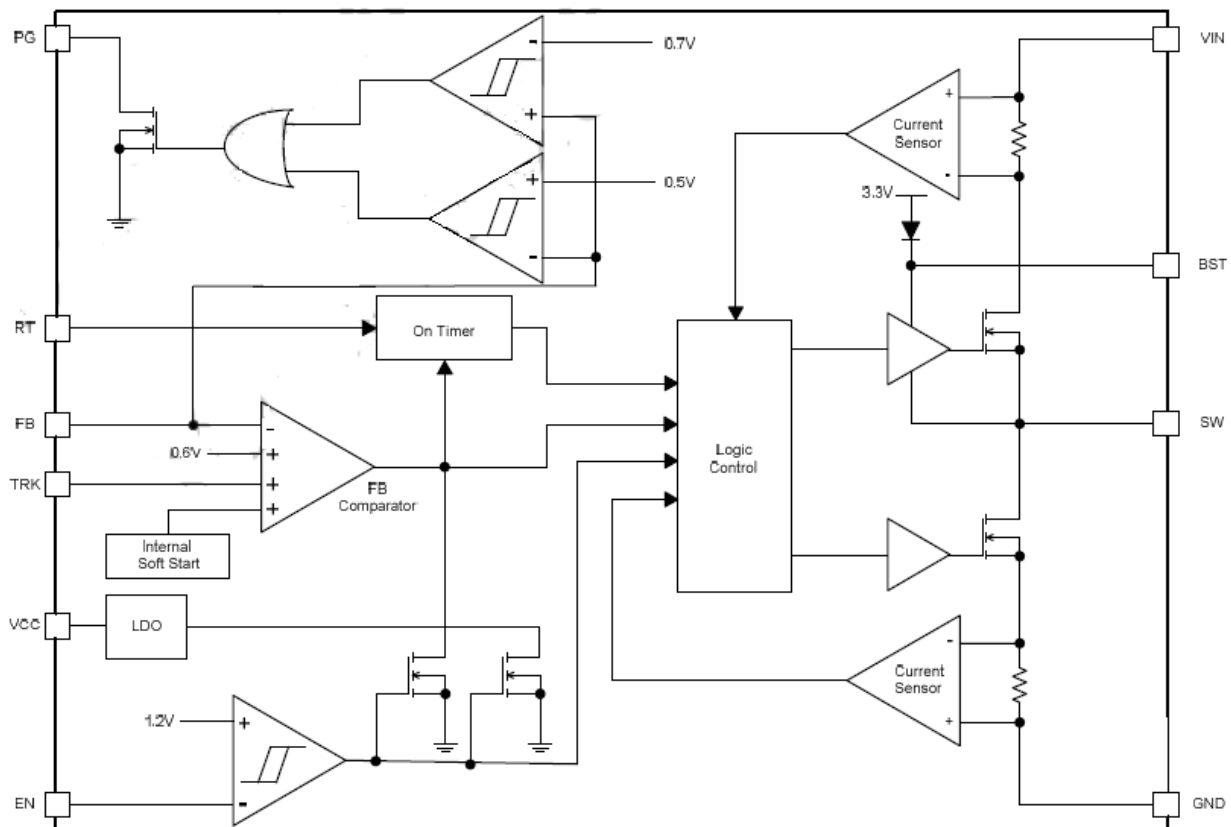
Typical Performance Characteristics

Vin=12V, Vout =1.8V, L=1.2μH, Cout=22μFX5, R6=330kΩ, C6=270pF, C7=100nF, TA = +25℃, unless otherwise noted

Steady State Test

VIN=12V, Vout=3.3V

Iout=8A
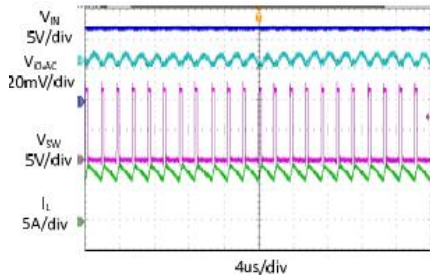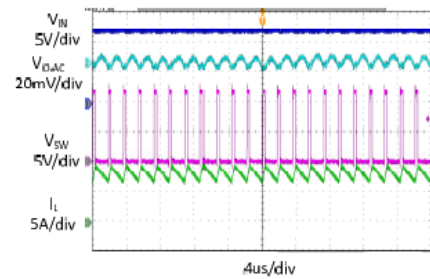
Startup through Enable

VIN=12V, Vout=3.3V

Iout=8A(Resistive load)
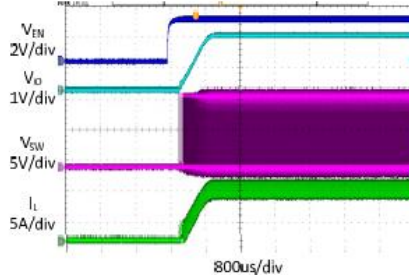
Shutdown through Enable
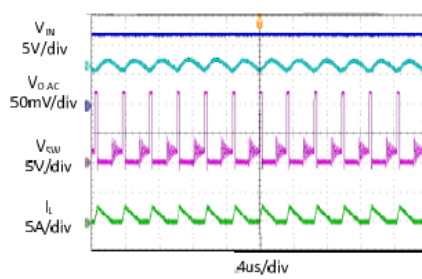
VIN=12V, Vout=3.3V

Iout=8A (Resistive load)
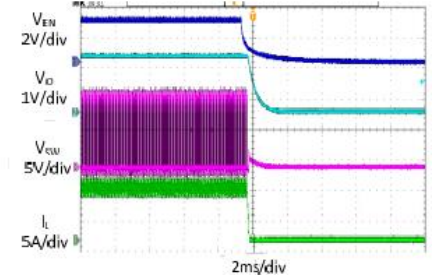
Heavy Load Operation

8A LOAD

Medium Load Operation
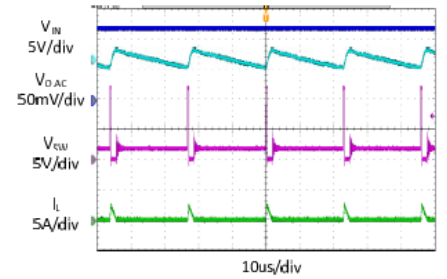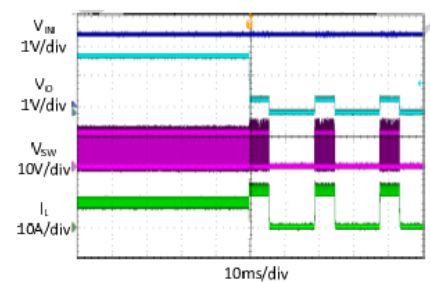
0.8A LOAD

Light Load Operation

0.1A LOAD

Short Circuit Protection

VIN=12V, Vout=3.3V

Iout= Short-8A

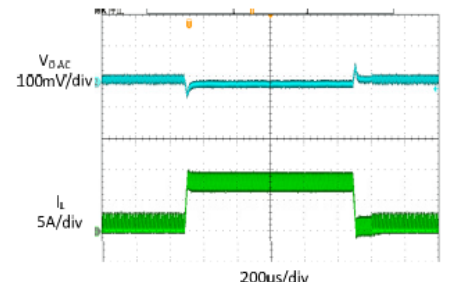**Short Circuit Recovery**

VIN=12V,Vout=3.3V

Iout= Short-8A
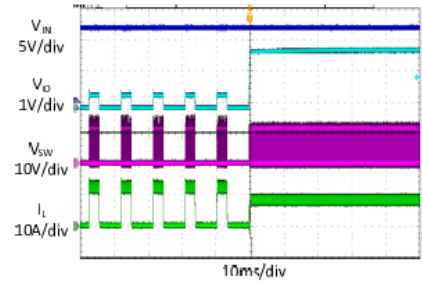
Load Transient

0.8A LOAD → 8A LOAD → 0.8A LOAD

Current slew rate: 2.5A/us @ R6=510 kΩ

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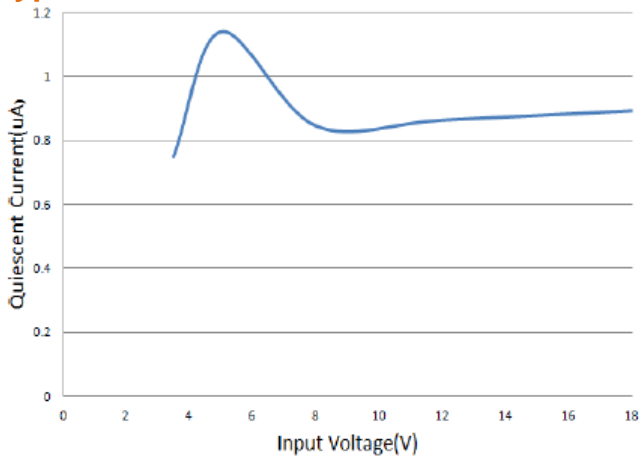## Typical Performance Characteristics (continued)
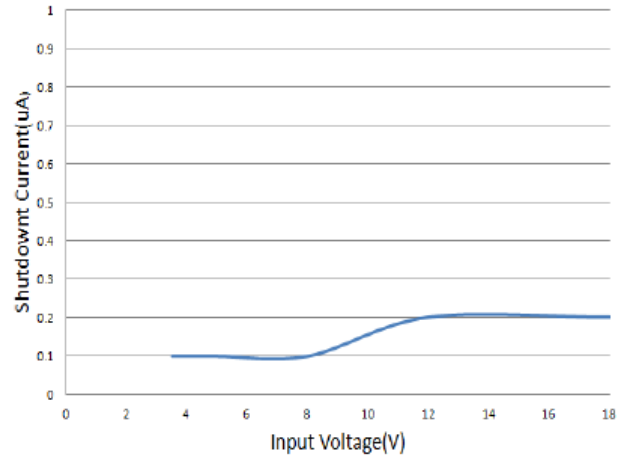

Figure 1. Shutdown Current vs Input Voltage

Figure 2. Supply Current vs Input Voltage
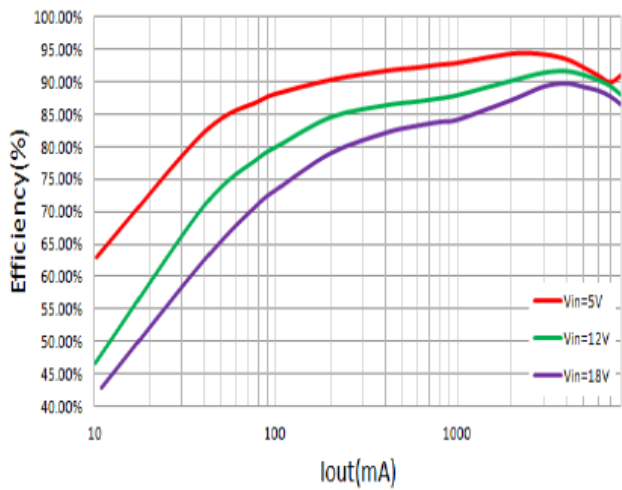

Figure 3. Efficiency vs Load Current (Vout=1.8V)

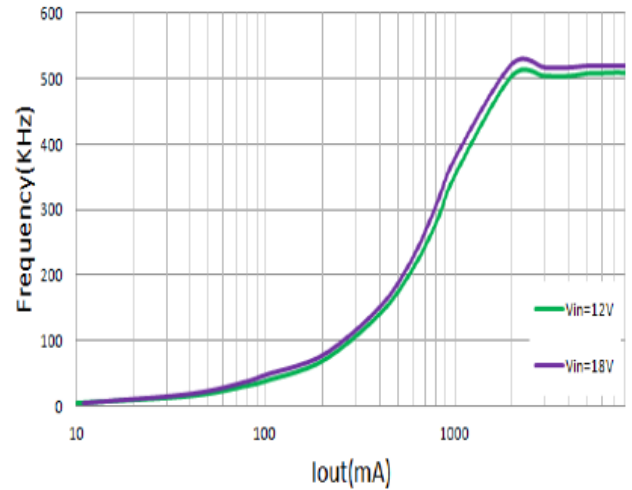Figure 4. Switching Frequency vs Load Current

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Functional Description

EJW5080 is a synchronous constant on-time step-down regulator. It regulates input voltages from 3.3V to 18V down to an output voltage as low as 0.6V, and is capable of supplying up to 8A of load current.

Stand-Alone Mode

EJW5080 can be set to operate as a stand-alone regulator by pulling the TRK pin to the VCC pin. In stand-alone mode, the regulator soft starts with the internal soft-start period of 1ms.

Tracking Mode

EJW5080 can be set to operate in tracking mode by connecting the TRK pin to the output of other regulators.   In tracking mode,
The output of EJW5080 follows the output of the tracked regulator to achieve certain power sequence.

Shut-Down Mode

EJW5080 shuts down when voltage at EN pin is driven below 0.3V. The entire regulator is off and the supply current consumed by EJW5080 drops below 1uA.

Power Switch

N-Channel MOSFET switches are integrated on the EJW5080 to down convert the input voltage to the regulated output voltage.
Since the top MOSFET needs a gate voltage greater than the input voltage, a boost capacitor connected between BST and SW pins is required to drive the gate of the top switch. The boost capacitor is charged by the internal 4V rail when SW is low.
Vin Under-Voltage Protection
A resistive divider can be connected between Vin and ground, with the central tap connected to EN, so that when Vin drops to the pre-set value, EN drops below 1.1V to trigger input under voltage lockout protection.

Hot-plug In Protection

No switching is allowed whenever the voltage at the Vin pin is higher than 21.6V. After hot-plug in protection is triggered, switching is not allowed until the Vin voltage drops below 18V.

Output Current Run-Away Protection

The current limit is decided by the maximum comp voltage which is around 2.5V. Comp voltage is also adjusted with the output current. The comp voltage decreases as load current drop. When comp voltage keeps the maximum value for around 12480 cycle, the over load protection is triggered. IC enters into the hiccup mode during the OLP.

Output Current Run-Away Protection

At start-up, due to the high voltage at input and low voltage at output, current inertia of the output inductor can be easily built up, resulting in a large start-up output current. A valley current limit is designed in JW5080 so that only when output current drops below the valley current limit can the top power switch be turned on. By such control mechanism, the output current at start-up is well controlled.

Output Short Protection

When the output is shorted to ground, the regulator is allowed to switch for 512 cycles. If the short condition is cleared within this period, then the regulator resumes normal operation. If the short condition is still present after 512 switching cycles, then no switching is allowed and the regulator enters hiccup mode for 2048 cycles. After the 2048 hiccup cycles, the regulator will try to start-up again. If the short condition still exists after 512 cycles of switching, the regulator enters hiccup mode. This process of start-up and hiccup iterate itself until the short condition is removed.

FB Short Protection

If the FB pin is detected to be short to ground, EJW5080 is not allowed to switch to prevent the output voltage from soaring high. The regulator can be reactivated again when the short condition at the FB pin is removed.

RT Short Protection

If the RT pin is detected to be short to ground, EJW5080 is not allowed to switch to prevent the output voltage from soaring high. The regulator can be reactivated again when the short condition at the RT pin is removed.

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Thermal Protection

When the temperature of the EJW5080 rises above 140°C, it is forced into thermal shut-down. Only when core temperature drops below 125°C can the regulator becomes active again.

Application Information

Output Voltage Set

The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:
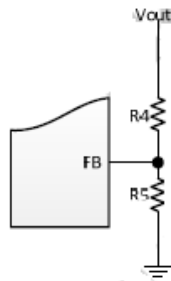
$$V_{FB} = V_{out} * \frac{R_5}{R_4 + R_5}$$

where VFB is the feedback voltage and VOUT is the output voltage.

Choose R_5 around $10k\Omega$, and then R4 can be calculated by:

$$R_4 = R_5 * \left(\frac{V_{out}}{0.6} - 1\right)$$

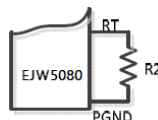Too large resistance and the following table lists the recommended values.

VOUT(V)	R5(kΩ)	R4(kΩ)
1	10	6.7
1.2	10	10
1.8	10	20
2.5	10	31.6
3.3	10	46.4

Operating Frequency

EJW5080 working frequency can be adjusted in different application. Set the resistor connected to RT pin to setup the working frequency as following expression.

$$Frequency = \frac{V_{out}}{10.5 * R_2 * 10^{-12}} \text{ Hz}$$

Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintaining the DC input voltage. The ripple current through the input capacitor can be calculated by:

$$I_{C1} = I_{LOAD} \cdot \sqrt{\frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

where ILOAD is the load current, VOUT is the output voltage, VIN is the input voltage. Thus the input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_1 = \frac{I_{LOAD}}{f_s \cdot \Delta V_{IN}} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where C1 is the input capacitance value, fs is the switching frequency, $\triangle$VIN is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimizing the potential noise, a small X5R or X7R ceramic capacitor, i.e. 0.1uF, should be placed as close to the IC as possible when using electrolytic capacitors.
A 44uF ceramic capacitor is recommended in typical application.

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Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_s \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot \left(R_{ESR} + \frac{1}{8 \cdot f_s \cdot C_2}\right)$$

where C2 is the output capacitance value and RESR is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, which lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system stability and transient response, and a 22uF*5 ceramic capacitor is recommended in typical application.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 40% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_s \cdot \Delta I_L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where VIN is the input voltage, VOUT is the output voltage, fs is the switching frequency, and IL is the peak-to-peak inductor ripple current.

External Bootstrap Capacitor

A bootstrap capacitor is required to supply voltage to the top switch driver. A 0.1uF low ESR ceramic capacitor is Recommended to connected to the BST pin and SW pin.

External voltage ripple injection

R6 C6 C7 there components are used to inject external ripple to FB. A Vp-p ripple is recommended to add to FB. R6 and C6 Are selected to choose the amplitude of external ripple. C7 couple the external ripple to FB.
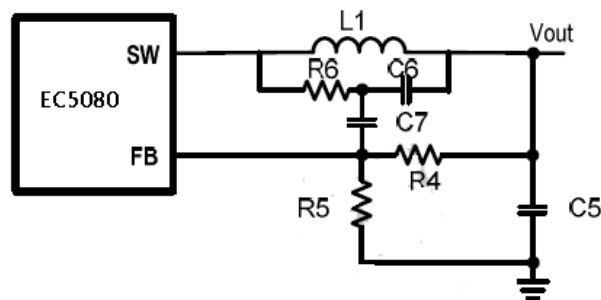
Vp-p ripple is recommended:

$$V_{ripple} = 17.5 * \sqrt{\frac{Vout}{Frequency}}$$

The external ripple can be calculated by:

$$V_{ripple} = \frac{(V_{in} - V_{out}) \cdot T_{on}}{R_6 * C_6}$$

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For best results, select a C7 value at least 10*C6 for better DC blocking performance, but smaller than 0.47Uf account for startup performance. Choose R6 around 330kΩ, C7 around 100nF and then C6 can be calculated by:

$$C_6 = \frac{(V_{in} - V_{out}).T_{on}}{V_{ripple} * C_6}$$

PCB Layout Note

For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. Place high current paths (GND, IN, and SW) very close to the device with short, direct and wide traces.
2. Put a decoupling capacitor as close to the VCC and AGND pins as possible.
3. Keep the switching node (SW) plane as small as possible and far away from the feedback network.
4. Place the external feedback resistors next to the FB pin. Make sure that there are no vias
5. Keep the BST voltage path (BST, C7, and SW) as short as possible.
6. R6 and C6 must be placed close to the on the FB trace. The feedback resistors should refer to AGND instead of PGND. inductor and C7 must be close to the IC.
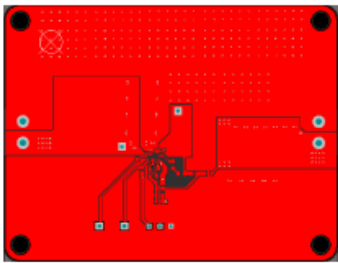7. Recommend strongly a four-layer layout to improve thermal performance
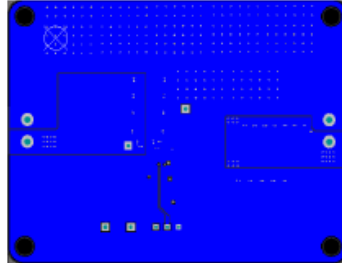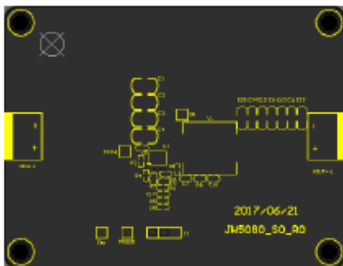

Figure 1. Top Layer

Figure 2. Bottom Layer

Figure 3. Top Silk Layer

External Components Suggestion @ Vin=12V:

VOUT(V)	R2 (kΩ)	R4 (kΩ)	R5 (kΩ)	R6(kΩ)	C6 (pF)	C7 (nF)	L1 (uH)	C5 (uF)
1	200	6.7	10	330	220	100	1	22*5
1.2	232	10	10	330	220	100	1	22*5
1.5	287	15	10	330	270	100	1	22*5
1.8	330	20	10	330	270	100	1.2	22*5
2.5	470	31.6	10	330	330	100	1.5	22*5
3.3	620	46.4	10	330	330	100	2.2	22*5

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External Components Suggestion @ Vin=5V:

VOUT(V)	R2 (kΩ)	R4 (kΩ)	R5 (kΩ)	R6(kΩ)	C6 (pF)	C7 (nF)	L1 (uH)	C5 (uF)
1	200	6.7	10	330	220	100	0.56	22*5
1.2	232	10	10	330	220	100	1	22*5
1.5	287	15	10	330	220	100	1	22*5
1.8	330	20	10	330	220	100	1	22*5
2.5	470	31.6	10	330	180	100	1	22*5
3.3	620	46.4	10	330	150	100	1	22*5
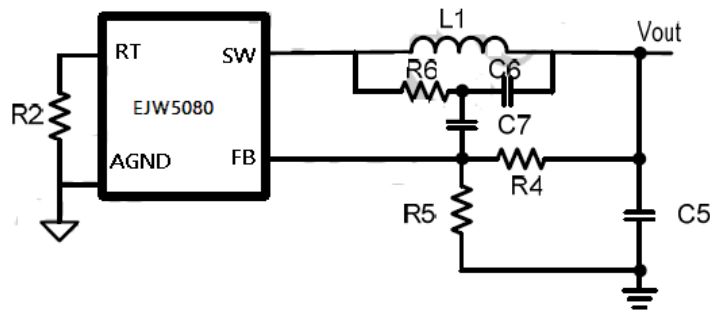
Reference Design

Reference 1:
Vin :4V~18V
Vout:1.8V
Iout :0~8A

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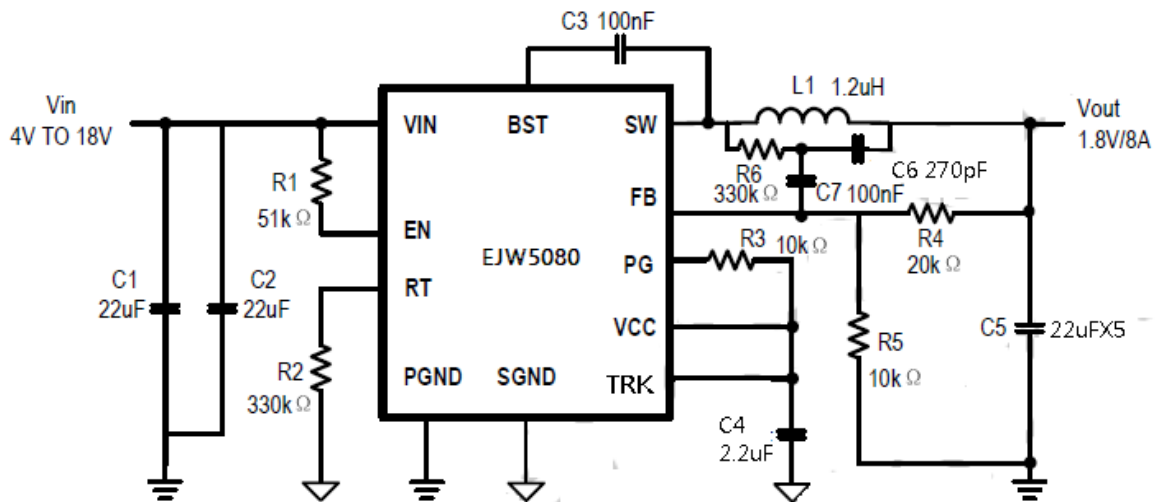
Package Outline
QFN3*4
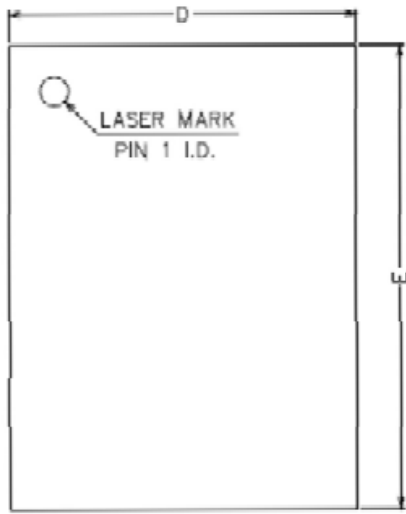
Top View

Side View
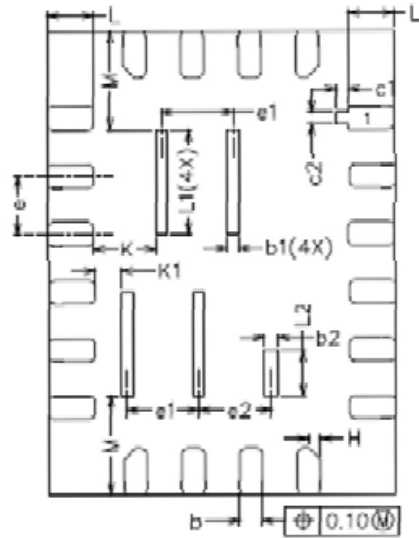
Bottom View
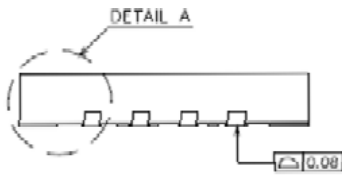
Side View
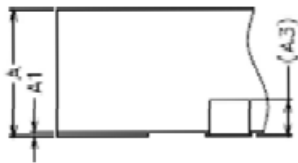
Detail A

Symbol	Dimensions In Millimeters		
	Min.	**Nom.**	**Max.**
A	0.50	0.55	0.60
A1	0.00	0.02	0.05
A3	0.15REF		
b	0.15	0.20	0.25
b1	0.05	0.10	0.15
b2	0.07	0.12	0.17
D	2.90	3.00	3.10
E	3.9	4.00	4.10
e	0.40	0.50	0.60
e1	0.52	0.62	0.72
e2	0.53	0.63	0.73
H	0.10REF		
K	0.44	0.54	0.64
K1	0.13	0.23	0.33
L	0.30	0.40	0.50
L1	0.80	0.90	1.00
L2	0.29	0.39	0.49
M	0.75	0.85	0.95
c1	-	0.10	-
c2	-	0.10	-

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