Features

◆Wide voltage operation
- 1.7V 5.5V supply

◆Two Wire Serial Interface,I 2 C TM Compatible
- Bi directional data transfer protocol

◆Speed
- 400 KHz(1.7V) and 1 MHz(2.5V 5.5V)

◆Low power consumption
- 0.5mA, 1.7V Operating current(max)
- 1uA, 1.7V Standby curr ent(max)

◆Hardware Data Protection
- Write Protect pin

◆Flexible Architecture
- Sequential&Random read features
- Memory organization: 65536 x 8 bits
- Page size:128 bytes

◆Advanced Feature
- Schmitt Trigger, filtered inputs for noise suppression
- Lockable 128 Byte security sector
- 128 Bit unique ID for each device
- Self time write cycles(5ms max)

◆High reliability
- Endurance: 1,000,000 write cycles
- Data retention: 40 years

◆Package Options
- PDIP8
- SOP8
- TSSOP8
- UDFN8

General Description

The EC24C256T provides 524,288 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 65,536 words of 8 bits each, with 128 bit UID and 128 byte Security Sector. The device's cascadable feature allows up to 8 devices to share a common 2 wire bus. The device is optimized for use in many industrial and commercial applications where low power and low voltage operations are essential.

Function Block Diagram

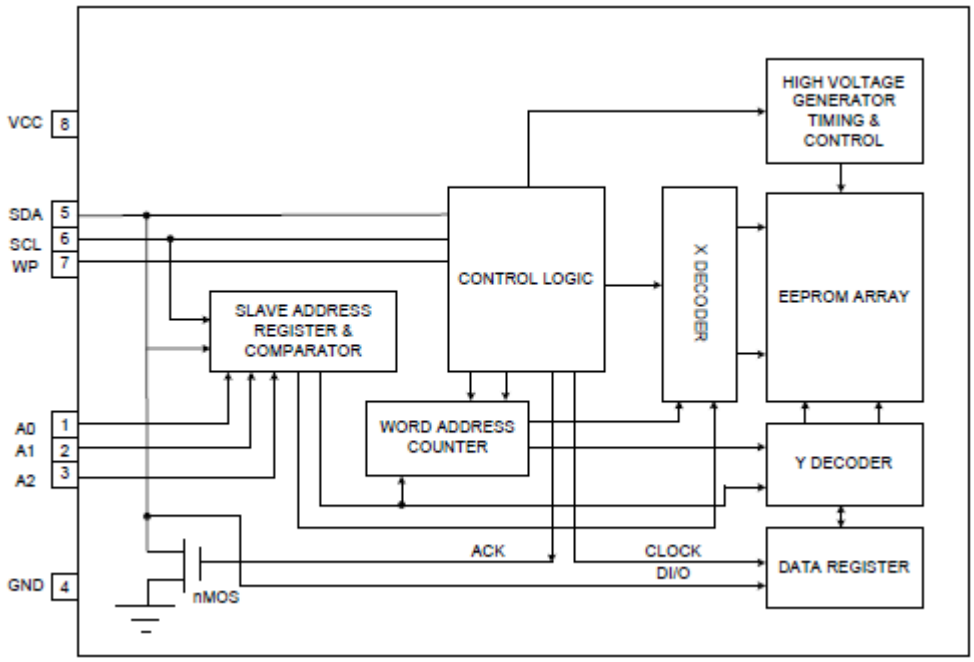


Figure 3.1 Block Diagram

Absolute Maximum Ratings

Table 4.1 Absolute Maximum Rating

Operating Temperature(Plastic Package)	-55℃ to +125 ℃
Operating Temperature(Module Package)	-20℃ to +60 ℃
Storage Temperature(Plastic Package)	-65℃ to +150 ℃
Storage Temperature(Module Package)	-25℃ to +70 ℃
Voltage on Any Pin with Respect to Ground	-1.0V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0mA

Note: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extend periods may affect device reliability.

Pin Configuration

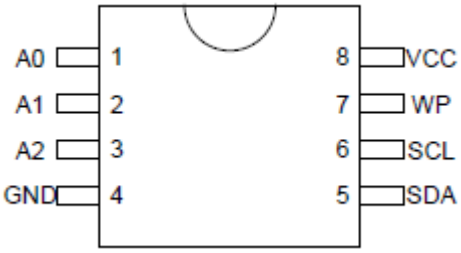


Figure 5.1 SOP8 and TSSOP

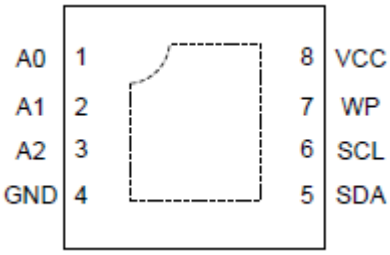


Figure 5.2 8-Lead UDFN

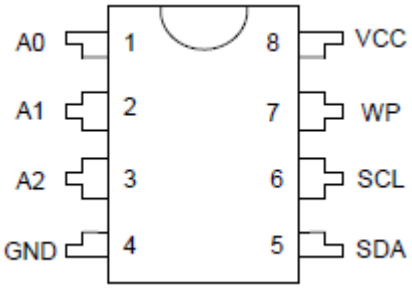


Figure 5.3 8-Pin PDIP

Table 5.1 Pin configuration

Pin Name	Function
A0-A2	Device Address Inputs
SDA	Serial Data Input/Output
SCL	Serial Clock Input
WP	Write Protect
Vcc	Power Supply
GND	Ground
NC	Not Connect

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each EEPROM device an negative edge clock data out of each device.

SERAIL DATA (SDA): The SDA pin is bi-directional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open-collector devices.

DEVICE/PAGE ADDRESSES(A2,A1,A0): The A2,A1 and A0 pins are device address inputs that are hardwired or left not connected for hardware compatibility with other T24CXX devices. When the pins are hardwired, as many as eight 256K devices may be addressed on a single bus system(device addressing is discussed in detail under the Device Addressing section). If the pins are left floating, the A2,A1 and A0 pins will be internally pulled down to GND if the capacitive coupling to the circuit board Vcc plane is <3pF, if coupling is >3pF, FSRK recommends connecting the address pins to GND.

WRITE PROTECT (WP): The EC24C256T has a Write Protect pin that provides hardware data protection. The WP pin allows normal write operations when connected to ground(GND). When the Write Protect pin is connected to VCC, all write operations to the memory are inhibited. If the pin is left floating, the WP pin will be internally pulled down to GND if the capacitive coupling to the circuit board Vcc plane is <3pF. If coupling is >3pF, FSRK recommends connecting the WP to GND. Switching WP to VCC prior to a write operation creates software write protected function.

Memory Organization

6.1. The memory is organized

EC24C256T, 256K SERIAL EEPROM: Internally organized with 256 pages of 128 bytes each, the 256K requires a 16-bit data word address for random word address.

Security sector: The EC24C256T offers 128 - byte Security Sectors which can be written and (later) permanently locked in Read-only mode. This memory may be used by the system manufacturers to store security and other important information separately from the main memory array.

Unique ID: The EC24C256T utilizes a separate memory block containing a factory programmed read-only 128-bit unique ID.

Table 6.1 The Memory Organization

Device ADDR	Page ADDR	Byte Number		
1010	0	127	...	0
	1	Data Memory (512P × 128B)		
	2			
	...			
	511			
1011	xxxx x00x xxxx xxxx(1)	Security Sector (128 Bytes)		
1011	xxxx xx1x xxxx xxxx(2)	Unique ID(128 Bits)		

Note: (1) Address bits ADDR<10:9> must be 00, ADDR<6:0> define byte address, other bits are don't care.

(2) Address bits ADDR<10:9> must be x1, ADDR<3:0> define byte address, other bits are don't care.

Device Operation

The EC24C256T serial interface supports communications using industrial standard 2-wire bus protocol, such as I2C.

7.1 2-WIRE Bus

The two-wire bus is defined as Serial Data (SDA), and Serial Clock(SCL). The protocol defines any device that sends data onto the SDA bus as a transmitter, and the receiving devices as receivers. The bus is controlled by Master device that generates the SCL, controls the bus access, and generates the Start and Stop conditions. The EC24C256T is the Slave device.

7.2 The Bus Protocol

The SDA pin is normally pulled high with an external device. Data on the SDA pin may change only during SCL low time periods(refer to Figure 7.5). Data changes during SCL high periods will indicate a start or stop condition as defined below.

7.3 Start Condition

A high-to-low transition of SDA with SCL high is a start condition which must precede any other command(refer to Figure 7.3).

7.4 Stop Condition

A low-to-high transition of SDA with SCL high is a stop condition. After a read sequence, the stop command will place the EEPROM in a standby power mode (refer to Figure 7.3).

7.5 Acknowledge

All address and data words are serially transmitted to and from the EEPROM in 8-bit words. The EEPROM sends a zero during the ninth clock cycle to acknowledge that it has received each word.

7.6 Reset

After an interruption in protocol, power loss or system reset, any 2-wire part can be reset in following these steps:
1. Clock up to 9 Cycles;
2 Look for SDA high in esch cycle while SCL is high and then;
3. Create a start condition as SDA is high.
The device should be ready for the next communication after above steps have been completed. In the event that the device is still non-responsive or remains active on the SDA bus, a power cycle must be used to reset the device.

7.7 Standby Mode

The EC24C256T features a low-power standby mode which is enabled:(a) upon power-up and (b) after the receipt of the stop bit and the completion of any internal operations.

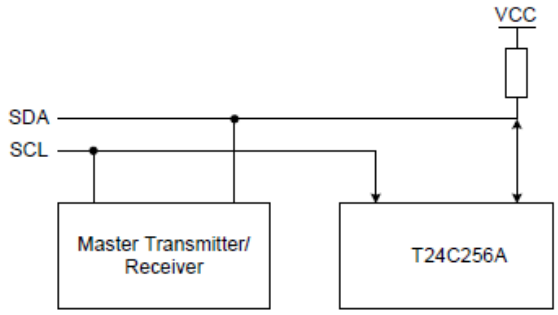


Figure 7.1 Typical System Bus Configuration

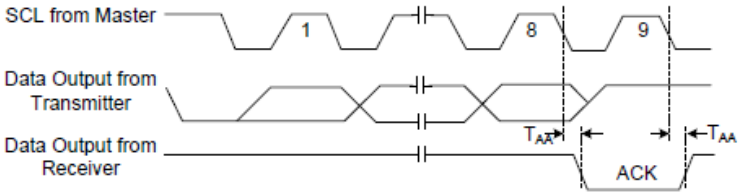


Figure 7.2 Output Acknowledge

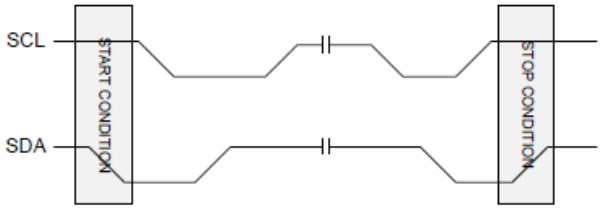


Figure 7.3 Start and Stop Conditions

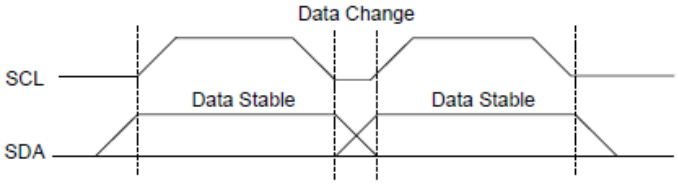


Figure 7.5 Data validity Protocol

Device Addressing

8.1 Data Memory Access

The 256K EEPROM requires an 8-bit device address word following a Start condition to enable the chip for a read or write operation. The device address word consists of a mandatory '1010' sequence for the first four most-significant bits (see Figure 8.1 below). This is common to all 2-wire EEPROM devices.

The 256K uses the three device address bits, A2, A1, and A0, to allow as many as eight devices on the same bus. These bits must compare to their corresponding hardwired input pins. The A2, A1, and A0 pins use an internal proprietary circuit that biases them to a logic low condition if the pins are allowed to float.

The eighth bit of the device address is the read/write operation select bit. A read operation is initiated if this bit is high, and a write operation is initiated if this bit is low.

Upon a compare of the device address, the EEPROM will output a zero. If a valid compare is not made, the device will return to a standby state.

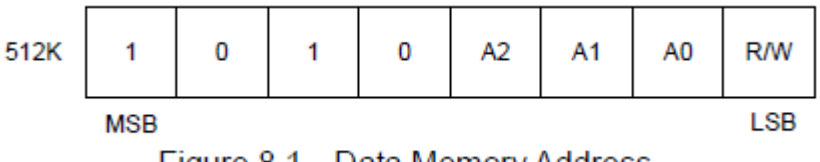


Figure 8.1 Data Memory Address

8.2 Unique ID Acess

The EC24C256T utilizes a separate memory block containing a factory programmed 128 -bi unique ID. Access to this memory location is obtained by beginning the device address word with a '1011'(Bh) sequence (refer to Table 8.1).The behavior of the next three bits(A2,A1 and A0) remains the same as during a standard memory addressing sequence.
The eighth bit of the device address needs be set to a one to read the Serial Number. Writing or altering the 128-bit unique ID is not possible.
For more details on accessing the special feature, See Read Operation on page 12.

8.3 Security Sector Access

The EC24C256T offers 128-byte Security Sector which can be written and (later) permanently locked in Read-only mode. Access to this memory location is obtained by beginning the device address word with a '1011'(Bh) sequence (refer to Table 8.1). The behavior of the next three bits (A2,A1 and A0) remains the same as during a standard memory addressing sequence.
The eight bit of the device address is the read/write operation is initiated if this bit is high and a write operation is initiated if this bit is low.
For more details on accessing this special feature, See Write Operations and Read Operation on page 10,13.

8.4 Noise Protection

Special internal circuitry placed on the SDA and SCL pins prevent small noise spikes from activating the device.

8.5 Data security

The Device has a hardware data protection scheme that allows the user to write protect the entire memory when the WP pin is at V_{CC}.

Table 8.1 Device Address

Access Area	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data Memory	1	0	1	0	A2	A1	A0	R/W
Security Sector	1	0	1	1	A2	A1	A0	R/W
Security Sector Lock Bit	1	0	1	1	A2	A1	A0	R/W
Unique ID Number	1	0	1	1	A2	A1	A0	1

Table 8.2 Frist Word Address

Access Area	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data Memory	A15	A14	A13	A12	A11	A10	A9	A8
Security Sector	x	x	x	x	x	0	0	x
Security Sector Lock Bit	x	x	x	x	x	1	0	x
Unique ID Number	x	x	x	x	x	x	1	x

Note:x represent don't care bit

Table 8.3 Second Word Address

Access Area	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
Data Memory	A7	A6	A5	A4	A3	A2	A1	A0
Security Sector	x	A6	A5	A4	A3	A2	A1	A0
Security Sector Lock Bit	x	x	x	x	x	x	x	x
Unique ID Number	x	x	x	x	0	0	0	0

Note:x represent don't care bit

Write Operations

9.1 Byte Write

A Byte Write operation requires two 8-bit data word addresses following the device address word and acknowledgment. Upon receipt of this address, the EEPROM will again respond with a zero, and then the part is to receive an 8-bit data word. Following receipt of the 8-bit data word, the EEPROM will output a zero. The addressing device, such as a microcontroller, then must terminate the write sequence with a Stop condition. At this time, the EEPROM enters an internally-timed write cycle, tWR, to the nonvolatile memory. All inputs are disabled during this write cycle, and the EEPROM will not respond until the write is complete (see Figure 9.1).

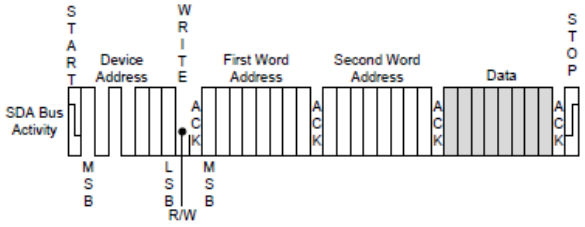


Figure 9.1 Byte Write

9.2 Page Write

A Page Write is initiated the same way as a byte write, but the microcontroller does not send a Stop condition after the first data word is clocked in. Instead, after the EEPROM acknowledges receipt of the first data word, the microcontroller can transmit up to 127 more data words. The EEPROM will respond with a zero after each data word received. The microcontroller must terminate the page write sequence with a Stop condition and the internally timed write cycle will begin. The lower seven bits of the data word address are internally incremented following the receipt of each data word. The higher data word address bits are not incremented, retaining the memory page row location. When the word address, internally generated, reaches the page boundary, the following byte is placed at the beginning of the same page. If more than 128 data words are transmitted to the EEPROM, the data word address will roll-over, and the previous data will be overwritten. The address roll over during write is from the last byte of the current page to the first byte of the same page (see Figure 9.2).

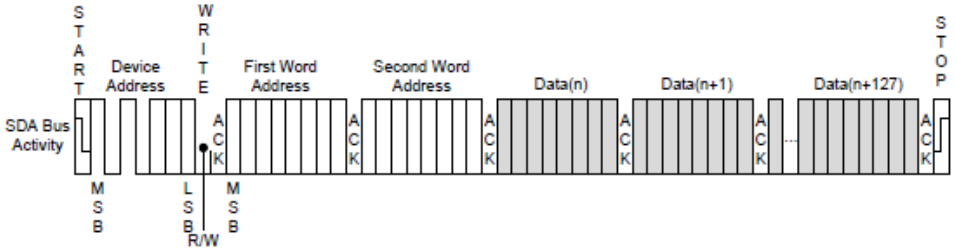


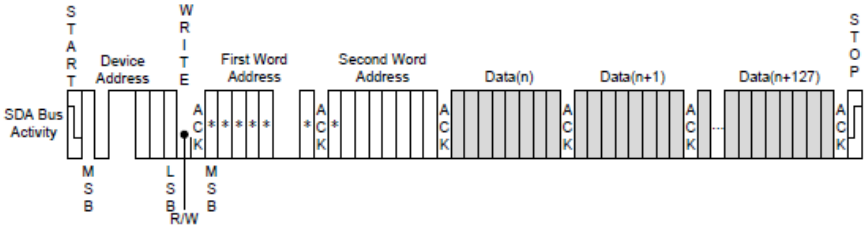
Figure 9.2 Page Write

9.3 Acknowledge Polling

Once the internally-timed write cycle has started and the EEPROM inputs are disabled, Acknowledge Polling can be initiated. This involves sending a Start condition followed by the device address word. The read/write select bit is representative of the operation desired. Only if the internal write cycle has completed will the EEPROM respond with a zero, allowing the read or write sequence to continue.

9.4 Write Security Sector

Write the Security sector is similar to the page write bur requires use of device address, and the special word address seen in Table 8.1. The higher address bits ADDR<15:7> are don't care except for address bits ADDR<10:9>, which must be equal to '00b'. Lower address bits ADDR<6:0> define the byte address inside the Security Sector (see Figure 9.3). If the Security Sector is locked, the data bytes transferred during the Write Security Sector operation are not acknowledge(NoAck).

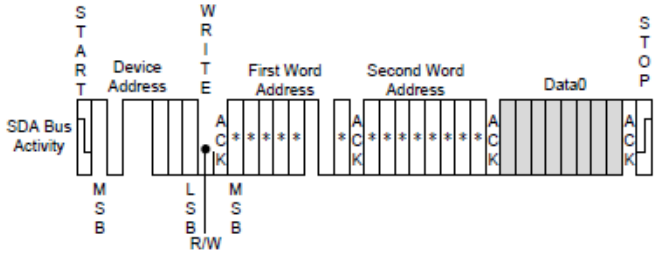


Note:1 *= Don't CARE bits

Figure 9.3 Write Security Sector

9.5 Lock Security Sector

Lock the Security Sector is similar to the byte write but requires use of device address, and special word address seen in Table 8.1. The word address bits ADDR<10:9> must be '10b', all other word address bits are don't care. The data byte must be equal to the binary value xxxx xx1x, where x is don't care (see Figure 14);
If the Security Sector is locked, the data bytes transferred during the Lock Security Sector operation are not acknowledged (NoAck).



Note:1 *= Don't CARE bits

Figure 9.4 Lock Security Sector

Read Operations

Read operations are initiated the same way as write operations with the exception that the read/write select bit in the device address word is set to one. There are three types of read operations: Current Address Read,Random Address Read, and Sequential Read.

10.1 Current Address Read

The internal data word address counter maintains the last address accessed during the last read or write operation, incremented by one. This address stays valid between operations as long as the chip power is maintained. The address roll-over during read is from the last byte of the last memory page to the first byte of the first page.
Once the device address with the read/write select bit set to one is clocked in and acknowledged by the EEPROM, the current address data word is serially clocked out on the SDA line. The microcontroller does not respond with an zero, but does generate a following Stop condition.

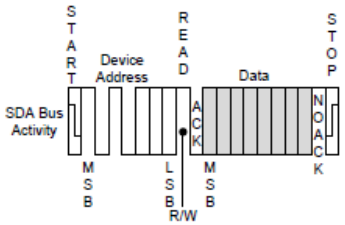


Figure 10.1 Current Address Read

10.2 Random Read

A Random Read requires an initial byte write sequence to load in the data word address. This is known as a "dummy write" operation. Once the device address word and data word address are clocked in and acknowledged by the EEPROM, the microcontroller must generate another Start condition. The microcontroller now initiates a current address read by sending a device address with the read/write select bit high. The EEPROM acknowledges the device address and serially clocks out the data word. The microcontroller does not respond with a zero, but does generate a following Stop condition.

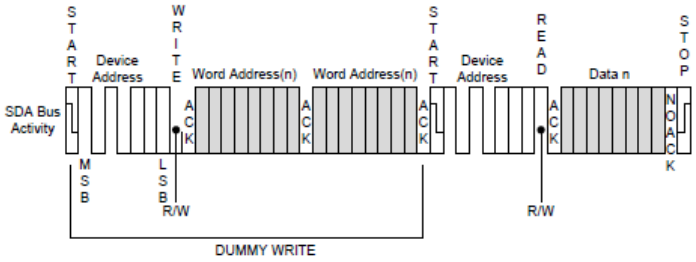


Figure 10.2 Random Read

10.3 Sequential Read

Sequential Reads are initiated by either a Current Address Read or a Random Address Read. After the microcontroller receives a data word, it responds with an acknowledge. As long as the EEPROM receives an acknowledge, it will continue to increment the data word address and serially clock out sequential data words. When the memory address limit is reached, the data word address will roll-over and the sequential read will continue. The Sequential Read operation is terminated when the microcontroller does not respond with a zero but does generate a following Stop condition.

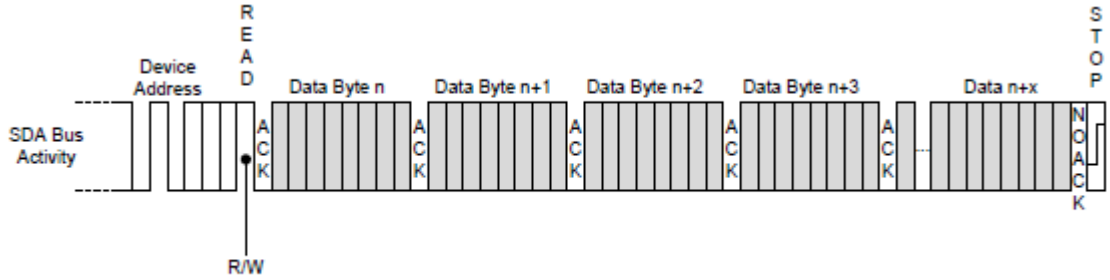
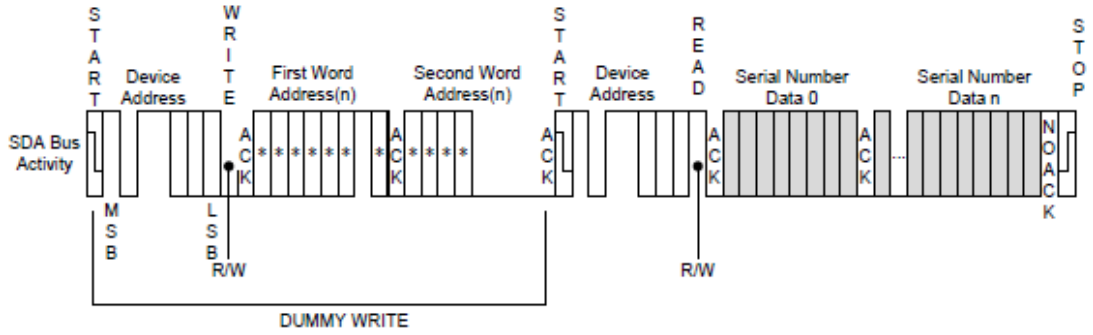


Figure 10.3 Sequential Read

10.4 Unique ID Read

Reading the serial number is similar to the sequential read but requires use of the device address, a dummy write, and the use of specific word address seen in Table 8.1. The higher address bits ADDR<15:4> are don't care except for address bits ADDR<10:9>, which must be equal to 'x1b', Lower address bits ADDR<3:0> define the byte address inside the UID. If the application desires to read the first byte of the UID, the lower address bits ADDR<3:0> would need to be '0000b'. When the end of the 128-bit UID number is reached(16 bytes of data), the data word address will roll-over back to the beginning of the 128-bit UID number. The Unique ID Read operation is terminated when the microcontroller does not respond with a zero (ACK) and instead issues a Stop condition (see Figure 10.4).



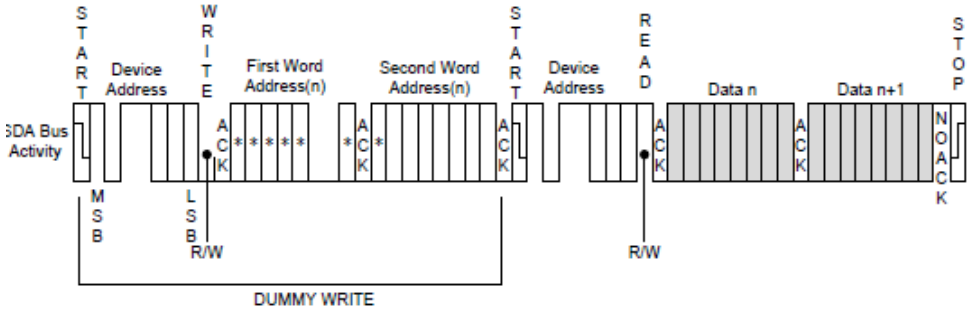
Note:1 *= Don't CARE bits

Figure 10.4 Read Unique ID

10.5 Read Security Sector

Read the Security Sector is similar to the random read but requires use of device address, a dummy write, and the use of specific word address seen in Table 1 on page 12. The higher address bits ADDR<15:7> are don't care except for address bits ADDR<10:9>, which must be equal to '00b'. The lower address bits ADDR<6:0> define the byte address inside the Security Sector.

The internal byte address is automatically incremented to the next byte address after each byte of data is clocked out. When the last byte (7Fh) is reached, it will roll over to 00h, the first byte of Security Sector, and continue to increment.(see Figure 10.5).

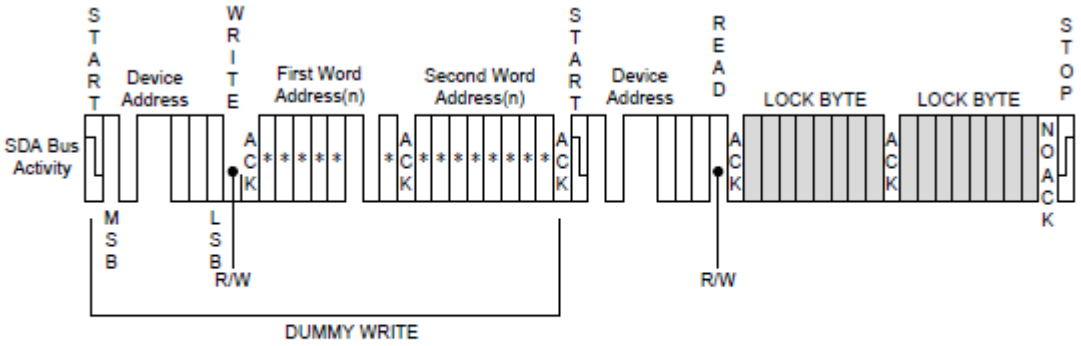


Note:1 *= Don't CARE bits

Figure 10.5 Read Security Sector

10.6 Read Lock Status

There are two ways to check the lock status of the Security Sector.
1. The first way is initiated by a Security Sector Write, the EEPROM will acknowledge if the Security Sector is unlock, while it will not acknowledge if the Security Sector is locked.
Once the acknowledge bit is read, it is recommended to generate a Start condition followed by a Stop condition, so that:
Start: the truncated command is not executed because the Start condition resets the device internal logic
Stop: the device is then set back into Standby mode by the Stop condition.
2. The second way is initiated by a Lock Status Read. Lock Status Read is similar to the random read but requires use of device address seen in Table 1 on page 12, a dummy write, and the use of specific word address. The address bits are Don't Care. The Lock bit is the BIT1 of the byte read on SDA. It is at "1" when the lock is active and at "0" when the lock is not active. The same data is shifted out repeatedly until the microcontroller does not respond with a zero but does generate a following stop condition(see Figure 10.6).



Note:1 *= Don't CARE bits

Figure 10.6 Read Lock Status

Electrical Characteristics

11.1 Absolute Maximum Ratings

Table 11.1 Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_S	Supply Voltage	-0.5 to +6.5	V
V_P	Voltage on Any Pin	-0.5 to V_{CC} +0.5	V
T_{BIAS}	Temperature Under Bias	-55 to +125	℃
T_{STG}	Storage Temperature	-65 to +150	℃
I_{OUT}	Output Current	5	mA

Note:Stress greater than those listed under Absolute Maximum Rating may cause permanent damage to device.This is a stress rating only an function operation of the device at these or any other condition outside those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

1.2 Pin Capacitance

Table 11.2 Pin Capacitance
Applicable over recommended operating range from TA = 25 C, f = 1.0MHz, VCC = 5.5V.

Symbol	Test Condition	Max	Units	Conditions
$C_{I/O}$	Input/Output Capacitance(SDA)	8	pF	$V_{I/O}$=0V
C_{IN}	Input Capacitance(A0,A1,A2,SCL)	6	pF	V_{IN}=0V

Note: 1. This parameter is characterized and is not 100% tested.

11.3 DC Characteristics

Table 11.3 DC Characteristics
Applicable over recommended operating range from: TAI = -40 ℃ to +85℃, VCC = 1.7V to 3.6V or 2.5V to 5.5V (unless otherwise noted).

Symbol	Parameter	Test Condition	Min	Typ	Max	Units
V_{CC}	Supply Voltage		1.7		5.5	V
$V_{IH(1)}$	Input High Voltage		0.7*Vcc		Vcc+0.5	V
$V_{IL(1)}$	Input Low Voltage		-0.6		0.3*Vcc	V
I_{LI}	Input Leakage Current	V_{IN}=V_{CC}/V_{SS}	-	0.1	3.0	uA
I_{LO}	Output Leakage Current	V_{IN}=V_{CC}/V_{SS}	-	0.05	3.0	uA
V_{OL1}	Output Low Voltage 1	V_{CC}=1.7V, I_{OL}=0.15 mA	-		0.2	V
V_{OL2}	Output Low Voltage 2	V_{CC}=3.0V, I_{OL}=2.1 mA	-		0.4	V
I_{SB1}	Standby Current	V_{CC}=1.7V, V_{IN}=Vcc/Vss			1.0	uA
I_{SB2}	Standby Current	V_{CC}=5.7V, V_{IN}=Vcc/Vss			6.0	uA
I_{CC1}	Supply Current	V_{CC}=5.0V, Read at 400KHz		0.4	1.0	mA
I_{CC2}	Supply Current	V_{CC}=5.0V, Write at 400KHz		2.0	3.0	mA

Note: (1) V_{IL} min and VIH max are reference only and are not tested.

11.4 AC Characteristics

Table 11.4 AC Characteristics(400 KHz characteristics)
Applicable over recommended operating range from T_A= -40 ℃ to +85 ℃, VCC = 1.7V to 2.5V (where applicable), CL = 100pF (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	Min	Max	Units
f_{SCL}	Clock Frequency, SCL		1	MHz
t_{LOW}	Clock Pulse Width Low	500		ns
t_{HIGH}	Clock Pulse Width High	320		ns
$t_{I(1)}$	Noise Suppression Time		80	ns
t_{AA}	Clock Low to Data Out Valid		450	ns
$t_{BUF(1)}$	Time the bus must be free before a new transmission can Start	500		ns
$t_{HD,STA}$	Start Hold Time	250		ns
$t_{SU,STA}$	Start Setup Time	250		ns
$t_{HD,DAT}$	Data In Hold Time	0		ns
$t_{SU,DAT}$	Data In Setup Time	50		ns
t_R	Inputs Rise Time(1)		120	ns
t_F	Inputs Fall Time(1)		120	ns
$t_{SU,STO}$	Stop Setup Time(1)	250		us
t_{DH}	Data Out Hold Time	100		ns
t_{WR}	Write Cycle Time		5	ms
Endurance	3.3V, 25 ℃, Page Mode	1,000,000		Write Cycles

11.5 AC Characteristics

Table 11.5 AC Characteristics(1 MHz AC characteristics)
Applicable over recommended operating range from T_A= 40 ℃ to +85℃, VCC = 2.5 V to 5.5V (where applicable), CL = 100pF (unless otherwise noted). Test conditions are listed in Note 2.

Symbol	Parameter	Min	Max	Units
f_{SCL}	Clock Frequency, SCL		1	MHz
t_{LOW}	Clock Pulse Width Low	500		ns
t_{HIGH}	Clock Pulse Width High	320		ns
$t_{I(1)}$	Noise Suppression Time		80	ns
t_{AA}	Clock Low to Data Out Valid		450	ns
$t_{BUF(1)}$	Time the bus must be free before a new transmission can Start	500		ns
$t_{HD,STA}$	Start Hold Time	250		ns
$t_{SU,STA}$	Start Setup Time	250		ns
$t_{HD,DAT}$	Data In Hold Time	0		ns
$t_{SU,DAT}$	Data In Setup Time	50		ns
t_R	Inputs Rise Time(1)		120	ns
t_F	Inputs Fall Time(1)		120	ns
$t_{SU,STO}$	Stop Setup Time(1)	250		us
t_{DH}	Data Out Hold Time	100		ns
t_{WR}	Write Cycle Time		5	ms
Endurance	3.3V, 25 ℃, Page Mode	1,000,000		Write Cycles

Note:
(1) This parameter is characterized and is not 100% tested.
(2) AC measurement conditions:
RL (connects to V_{CC}): 1.3KΩ
Input pulse voltages: 0.3 VCC to 0.7 V_{CC}
Input rise and fall times: ≤50ns
Input and output timing reference voltages:0.5 V_{CC}

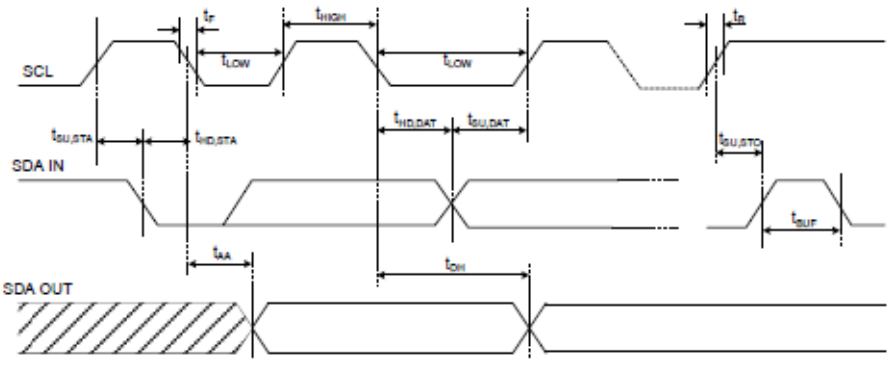


Figure 11.1 Bus Timing

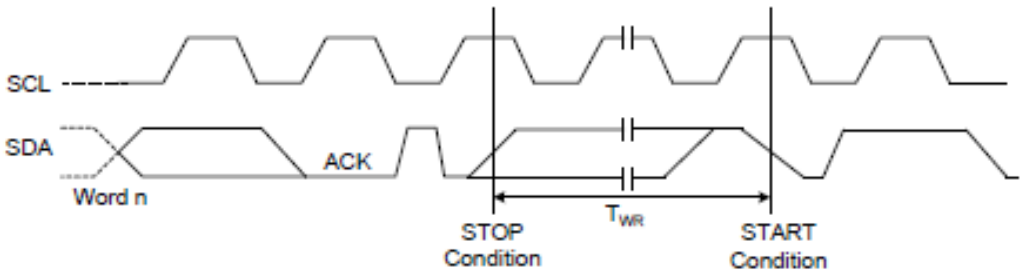
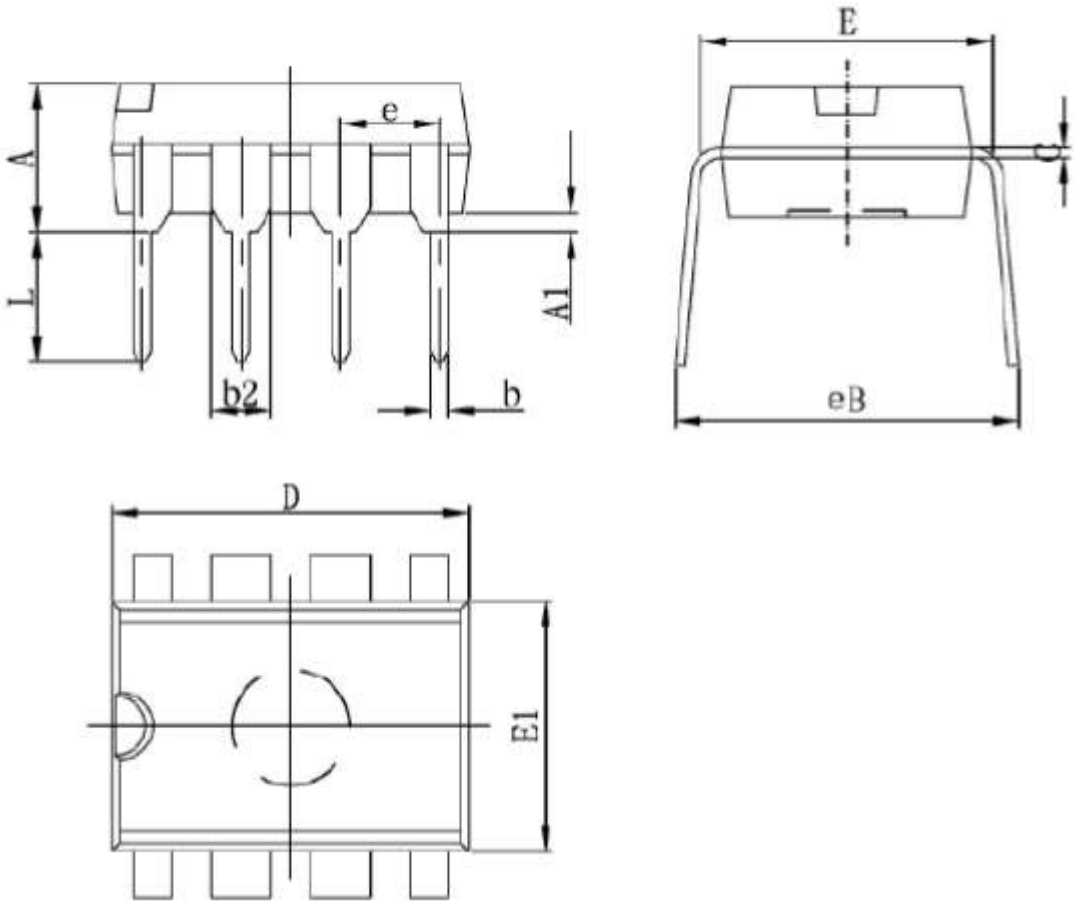


Figure 11.2 Write Cycle Timing

Part Markings

12.1 PDIP8

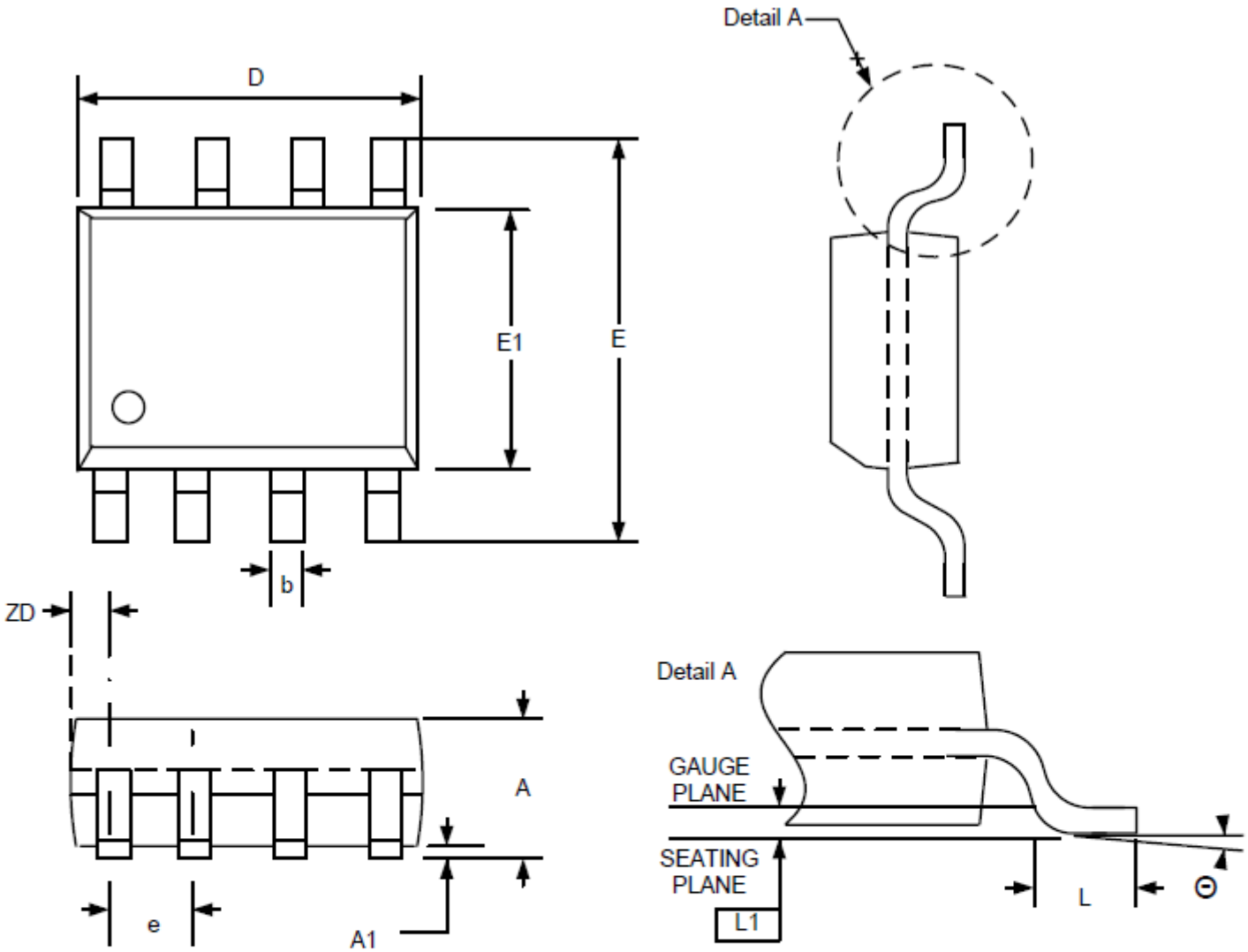


Symbol	MIN	MAX
A	---	5.000
A1	0.380	---
b	0.380	0.570
b2	1.300	1.700
C	0.200	0.360
D	9.000	10.000
E1	6.100	7.000
E	7.320	8.250
e	2.540(BSC)	
L	2.920	3.810
eB	---	10.900

NOTE:
1. Dimensions are in Millimeters.

12.2 SOP8

8L 150mil SOP Package Outline



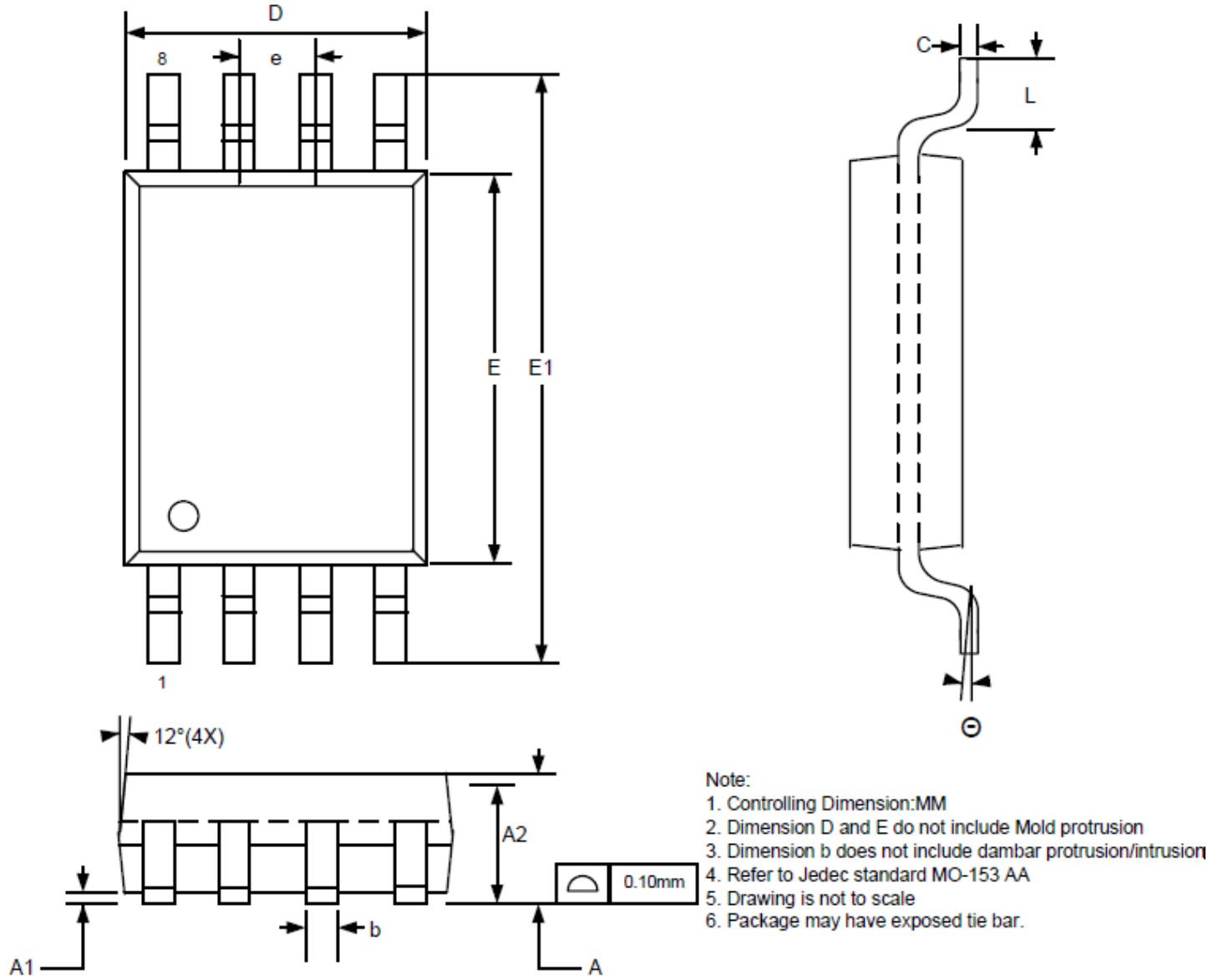
SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	--	1.75	0.053	--	0.069
A1	0.10	--	0.25	0.004	--	0.010
b	0.33	--	0.51	0.013	--	0.020
D	4.80	--	5.00	0.189	--	0.197
E	5.80	--	6.20	0.228	--	0.244
E1	3.80	--	4.00	0.150	--	0.157
e	1.27 BSC.			0.050 BSC.		
L	0.38	--	1.27	0.015		0.050
L1	0.25 BSC.			0.010 BSC.		
ZD	0.545 REF.			0.021 REF.		
Θ	0	--	8°	0	--	8°

Note:

1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion.
4. Refer to Jedec standard MS-012
5. Drawing is not to scale

12.3 TSSOP

8L 3x4.4mm TSSOP Package Outline

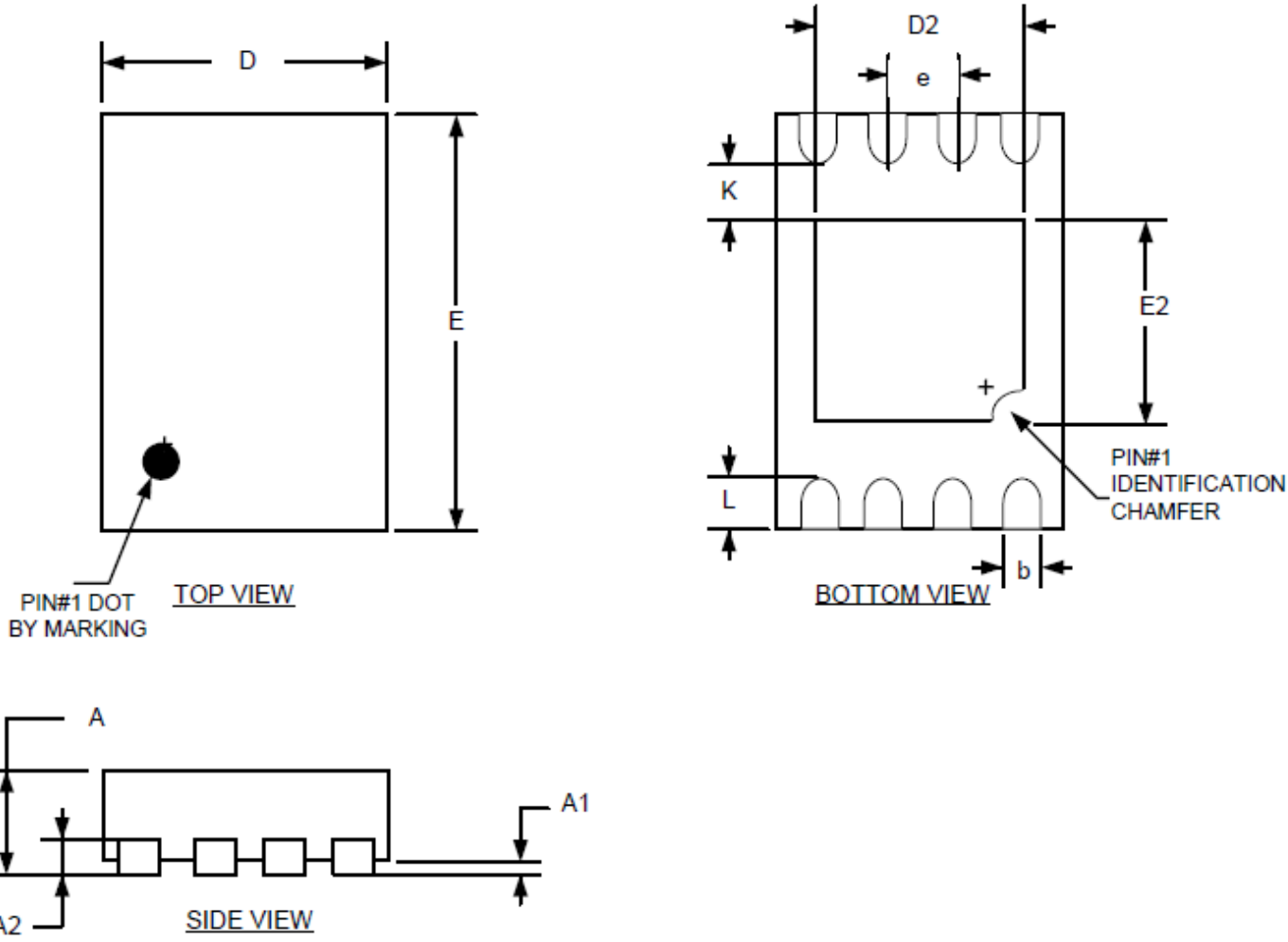


Note:
1. Controlling Dimension:MM
2. Dimension D and E do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion
4. Refer to Jedec standard MO-153 AA
5. Drawing is not to scale
6. Package may have exposed tie bar.

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.20	--	--	0.047
A1	0.05	--	0.15	0.002	--	0.006
A2	0.80	1.00	1.05	0.031	0.039	0.041
b	0.19	--	0.30	0.007	--	0.012
c	0.09	--	0.20	0.004	--	0.008
D	2.90	3.00	3.10	0.114	0.118	0.122
E	4.30	4.40	4.50	0.169	0.173	0.177
E1	6.4 BSC			0.252 BSC		
e	0.65 BSC			0.026 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
Θ	0	--	8°	0	--	8°

12.4 UDFN

8L 2x43mm UDFN Package Outline

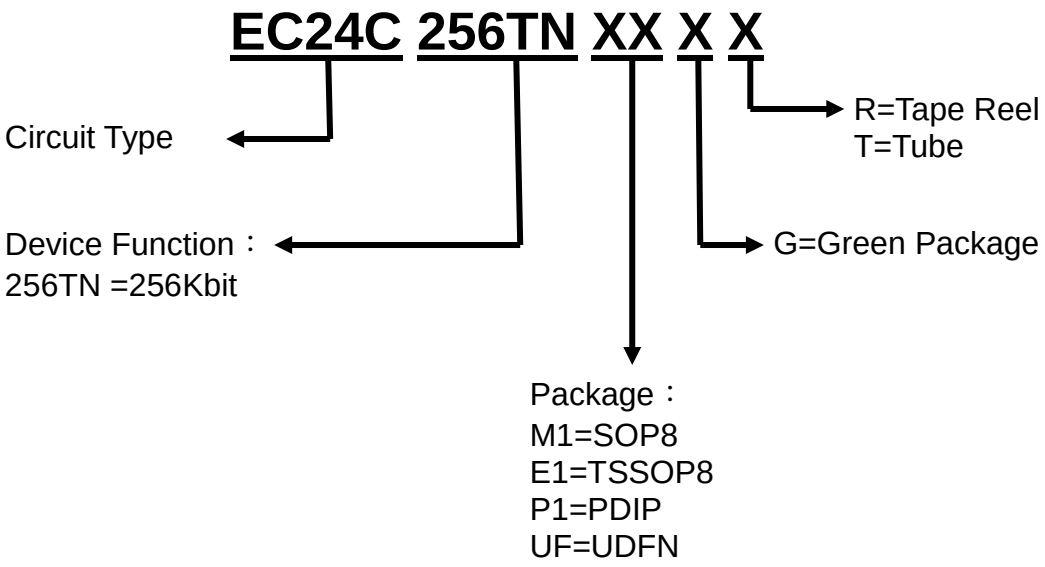


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.00	--	0.05	0.000	--	0.002
b	0.18	0.25	0.30	0.007	0.010	0.012
A2	0.152 REF			0.006 REF		
D	2.00 BSC			0.079 BSC		
D2	1.25	1.40	1.50	0.049	0.055	0.059
E	3.00 BSC			0.118 BSC		
E2	1.15	1.30	1.40	0.045	0.051	0.055
e	0.50 BSC.			0.020 BSC.		
K	0.40	--	--	0.016	--	--
L	0.20	0.30	0.40	0.008	0.012	0.016

Note:

1. Controlling Dimension:MM
2. Drawing is not to scale

Ordering / Marking Information



Marking	Marking Information
T24C256A YYWXX	YY is: Year Code (2020=20) W is: Date Code (A~Z=1~26weeks；a~z=27~52weeks) XX is Tracking Code