General Description

The EC3282S is a monolithic synchronous buck regulator. The device integrates 95mΩ MOSFETS that provide 2A Continuous load current over a wide operating input voltage of 4.5Vto 28V.Current mode control provides fast transient response and cycle-by-cycle current limit. An adjustable soft-start prevents inrush current at turn on.

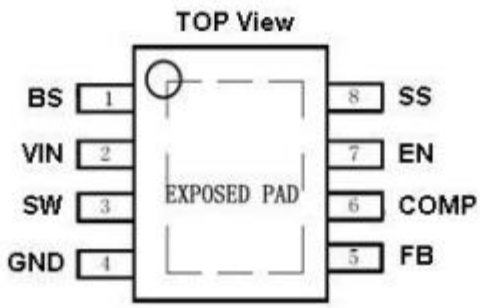
Features

- 2A Output Current
- Wide 4.5V to 28V Operating Input Range
- Output Adjustable from 0.925V to 0.8*VIN
- Up to 96 Efficiency
- Programmable Soft-Start
- Stable with Low ESR Ceramic Output Capacitors
- Fixed 340KHz Frequency
- Cycle-by-Cycle Over Current Protection
- Short-Circuit Protection
- Input Under Voltage Lockout
- Package：SOP 8L

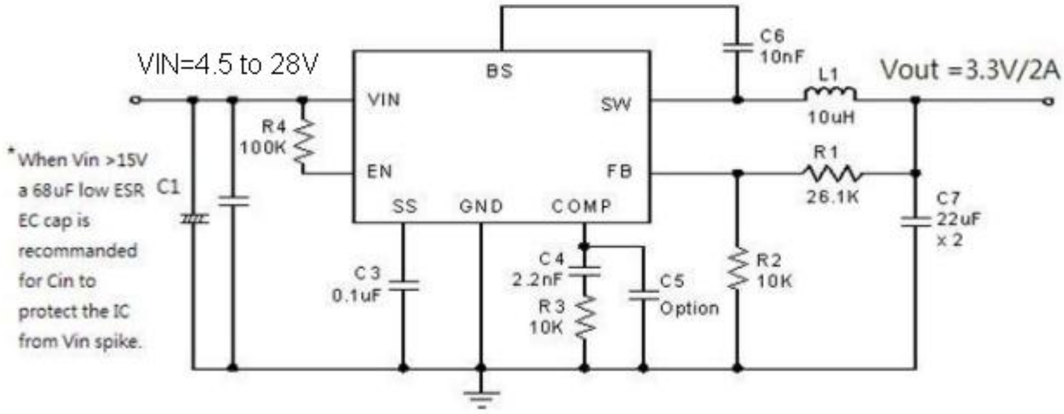
Applications

- Distributed Power Systems
- Networking Systems
- FPGA, DSP, ASIC Power Supplies
- Green Electronics/ Appliances
- Notebook Computers

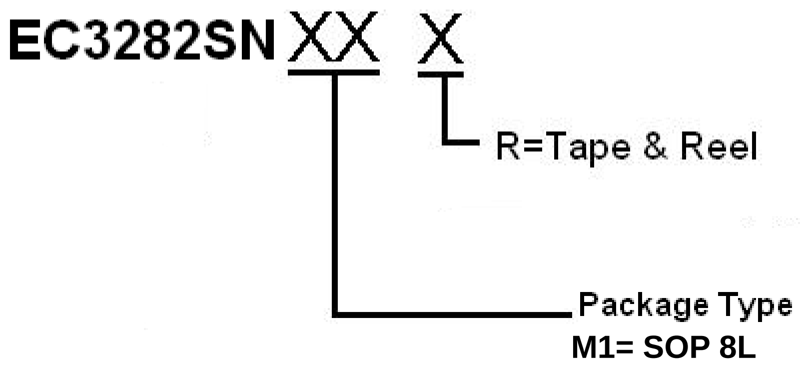
Pin Configurations



Typical Applications

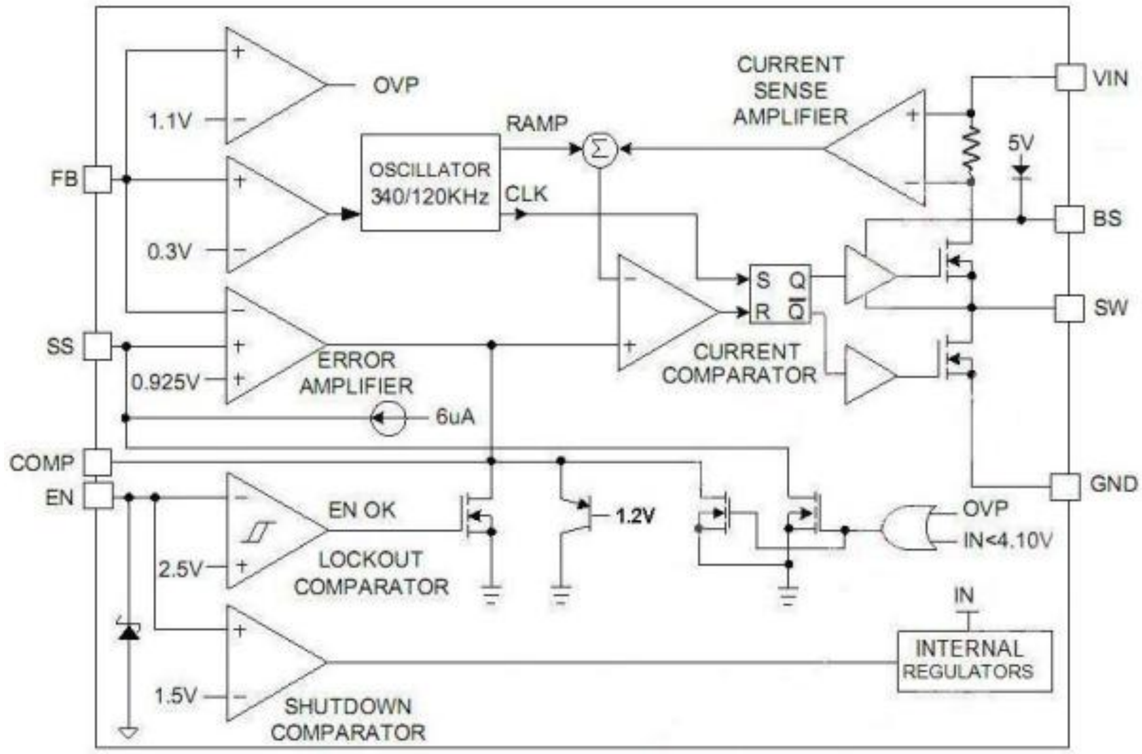


Ordering Information



Part Number	Package	Marking	Marking Information
EC3282SNM1R	SOP 8L	3282S LLLLL YYWWT	LLLLL is Lot Number YYWW is date code T is internal tracking code

Function Block



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage	V_{IN}	-0.3 to 30	V
SW Voltage	V_{SW}	-0.3 to V_{IN}+0.3	V
BS Voltage	V_{BS}	V_{SW} – 0.3V to V_{SW}+6	V
EN / FB / COMP Voltage		-0.3 to 5	V
Continuous SW Current		Internally limited	A
Operating Junction Temperature	T_J	150	ºC
Storage Temperature	T_{STG}	-65 to 150	ºC
Power Dissipation	P_D	Internally limited	W
Thermal Resistance-Junction to Ambient	θ_{JA}	87	ºC / W

Note: Exceeding these limits may damage the device. Even the duration of exceeding is very short. Exposure to absolute maximum rating conditions for long periods may affect device reliability。

Recommended Operating Conditions

Parameter	Symbol	Value	Units
Supply Input Voltage	V_{IN}	4.5 to +28	V
Operating Junction Temperature	T_J	-20 to +125	°C

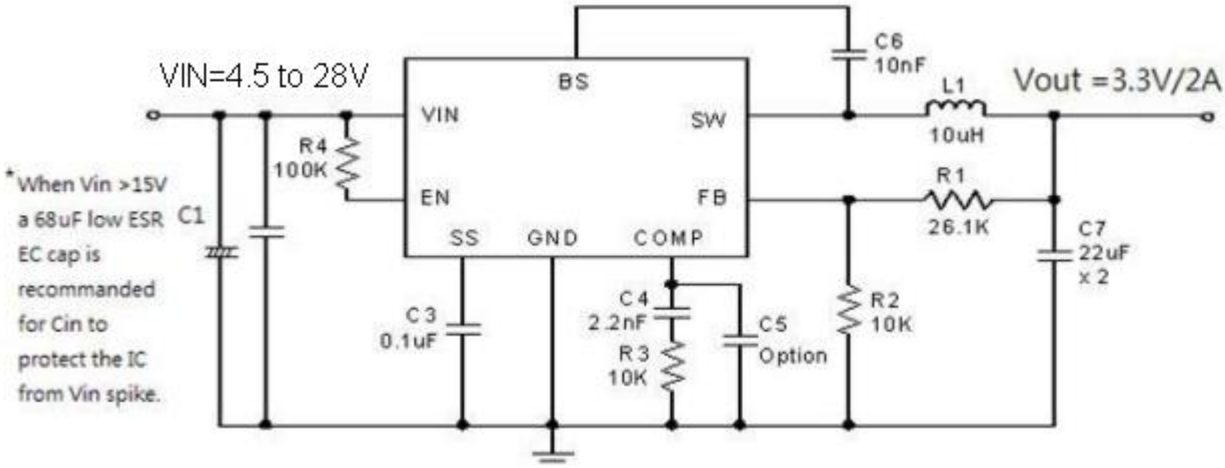
Electrical Characteristics

(V_{IN} = 12V, T_J = 25℃ unless otherwise specified.)

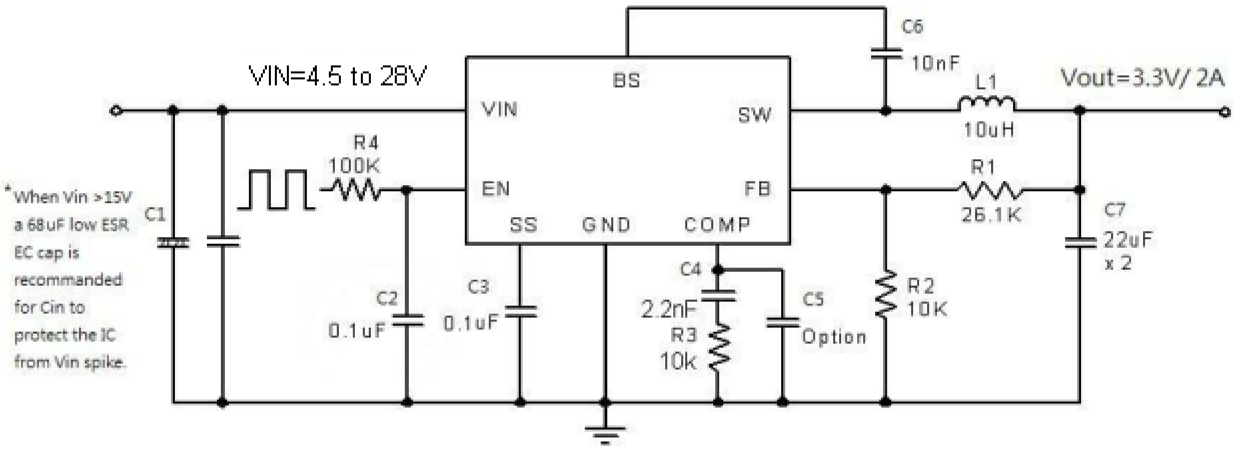
Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Feedback Voltage	V_{FB}	4.5V ≤ V_{IN} ≤ 28V	0.9	0.925	0.95	V
Feedback Overvoltage Threshold				1.1		V
High-Side Switch-On Resistance*				95		mΩ
Low-Side Switch-On Resistance*				95		mΩ
High-Side Switch Leakage		V_{EN} = V_{SW} = 0V	,		10	uA
Upper Switch Current Limit*		Min Duty Cycle	2.7	3.5		A
COMP to Current Limit Trans conductance	G_{COMP}			3.3		A/V
Error Amplifier Trans conductance	G_{EA}	ΔI_{COMP} = ±10uA		920		uA/V
Error Amplifier DC Gain*A	V_{EA}			480		V/V
Switching Frequency	f_{SW}			340		KHz
Short Circuit Switching Frequency		V_{FB} = 0V		120		KHz
Maximum Duty Cycle	D_{MAX}	V_{FB} = 0.8V		92		%
Minimum On Time*				220		nS
EN Shutdown Threshold Voltage		V_{EN} Rising	1.1	1.4	2	V
EN Shutdown Threshold Voltage Hysteresis				180		mV
EN Lockout Threshold Voltage			2.2	2.5	2.7	V
EN Lockout Hysteresis				130		mV
Supply Current in Shutdown		V_{EN} = 0V		0.3	3	uA
IC Supply Current in Operation		V_{EN} = 3V, V_{FB}=1.0V		1.3	1.5	mA
Input UVLO Threshold Rising	UVLO	V_{EN} Rising	3.8	4.05	4.4	V
Input UVLO Threshold Hysteresis				100		mV
Soft-start Current		V_{SS} = 0V		6		uA
Soft-start Period		C_{SS} =0.1uF		15		mS
Thermal Shutdown Temperature*		Hysteresis =25°C		160		℃

Note: * Guaranteed by design, not tested

Typical Applications



EC3282S Circuit, 3.3V/2A output



EC3282S Circuit, 3.3V/2A output with EN function

Note: C2 is required for separate EN signal.

Applications

Output Voltage Setting

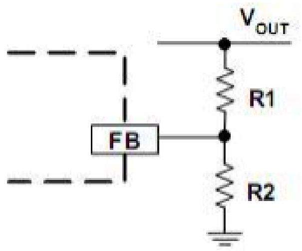


Figure1. Output Voltage Setting

Figure 1 shows the connections for setting the outputvoltage. Select the proper ratio of the two feedbackresistors R1 and R2 based on the output voltage.Typically, use R2≈10KΩ and determine R1 from the following equation:

$$R1 = R2\left(\frac{V_{OUT}}{0.925V} - 1\right) \quad (1)$$

Table1－Recommended Resistance Values：

VOUT	R1	R2
1V	1.0KΩ	12KΩ
1.2V	3.0KΩ	10KΩ
1.8V	9.53KΩ	10KΩ
2.5V	16.9KΩ	10KΩ
3.3V	26.1KΩ	10KΩ
5V	44.2KΩ	10KΩ
12V	121KΩ	10KΩ

Inductor Selection

The inductor maintains a continuous current to the output load. This inductor current has a ripple that is dependent on the inductance value: higher inductance reduces the peak-to-peak ripple current. The trade off for high inductance value is the increase in inductor core size and series resistance, and the reduction in current handling capability. In general,L based on the ripple current requirement:

$$L = \frac{V_{OUT} \bullet (V_{IN} - V_{OUT})}{V_{IN} f_{SW} I_{OUTMAX} K_{RIPPLE}} \quad (2)$$

Where VIN is the input voltage, VOUT is the output voltage,f_{SW} is the switching frequency, IOUTMAX is the maximumoutput current, and KRIPPLE is the ripple factor. Typically,choose KRIPPLE =~ 30% to correspond to the peak-to-peak ripple current being ~30% of the maximum output current. With this inductor value,the peak inductor current is $I_{OUT} \cdot (1+K_{RIPPLE}/2)$. Make sure that this peak inductor current is less than the upper switch current limit.

Finally, select the inductor core size so that it does not saturate at the current limit. Typical inductor values for various output voltages are shown in Table 2.

Table 2. Typical Inductor Values

V_{OUT}	1V	1.2V	1.8V	2.5V	3.3V	5V	9V
L	4.7uH	4.7uH	10uH	10uH	10uH	10uH	22uH

Input Capacitor

The input capacitor needs to be carefully selected to maintain sufficiently low ripple at the supply input of the converter. A low ESR Electrolytic (EC) capacitor is highly recommended. Since large current flows in and out of this capacitor during switching, its ESR also affects efficiency.When EC cap is used, the input capacitance needs to be equal to or higher than 68uF. The RMS ripple current rating needs to be higher than 50% of the output current. The input capacitor should be placed close to the VIN and GND pins of the IC, with the shortest traces possible. The input capacitor can be placed a little bit away if a small parallel 0.1uF ceramic capacitor is placed right next to the IC.

When Vin is >15V, pure ceramic Cin (* no EC cap) is not recommended. This is because the ESR of a ceramic cap is often too small, Pure ceramic Cin will work with the parasite inductance of the input trace and forms a Vin resonant tank.When Vin is hot plug in/out, this resonant tank will boost the Vin spike to a very high voltage and damage the IC.

Output Capacitor

The output capacitor also needs to have low ESR to keep low output voltage ripple.In the case of ceramic output capacitors,R_{ESR} is very small and does not contribute to the ripple. Therefore, a lower capacitance value can be used for ceramic capacitors.In the case of tantalum or electrolytic capacitors,the ripple is dominated byR_{ESR} multiplied by the ripple current. In that case, the output capacitor is chosen to have sufficiently low ESR.
For ceramic output capacitors, typically choose of about 22uF. For tantalum or electrolytic capacitors, choose a capacitor with less than 50mΩ ESR.

Optional Schottky Diode

During the transition between high-side switch and low-side switch, the body diode of the low side power MOSFET conducts the inductor current. The forward voltage of this body diode is high. An optional Schottky diode may be paralleled between the SW pin and GND pin to improve overall efficiency.

Stability Compensation

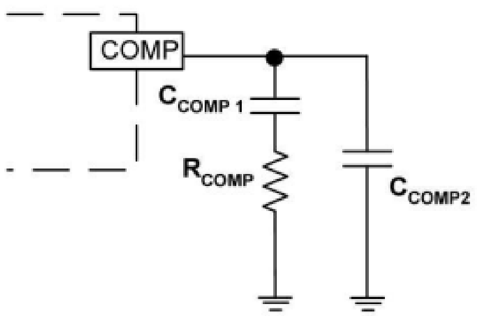


Figure 2. Stability Compensation

C_{COMP2} is needed only for high ESR output capacitor.

The feedback loop of the IC is stabilized by the components at the COMP pin, as shown in Figure 2. The DC loop gain of the system is determined by the following equation:

$$A_{VDC} = \frac{0.925\,V}{I_{OUT}} A_{VEA} G_{COMP} \qquad (4)$$

The dominant pole P1 is due to $C_{COMP}1$:

$$f_{P1} = \frac{G_{EA}}{2\pi A_{VEA} C_{COMP1}} \qquad (5)$$

The second pole P2 is the output pole:

$$f_{P2} = \frac{I_{OUT}}{2\pi V_{OUT} C_{OUT}} \qquad (6)$$

The first zero Z1 is due to R_{COMP} and C_{COMP}:

$$f_{Z1} = \frac{1}{2\pi R_{COMP} C_{COMP1}} \qquad (7)$$

And finally, the third pole is due to R_{COMP} and C_{COMP2} (if C_{COMP2} is used):

$$f_{P3} = \frac{1}{2\pi R_{COMP} C_{COMP2}} \qquad (8)$$

The following steps should be used to compensate the IC:

STEP1. Set the crossover frequency at 1/10 of the switching frequency via RCOMP: but limit R_{COMP} to 10KΩ maximum. More than 10 KΩ is easy to cause overshoot at power on.

$$R_{COMP} = \frac{2\pi V_{OUT} C_{OUT} f_{SW}}{10 G_{EA} G_{COMP} \bullet 0.925V} \qquad (9)$$

STEP2. Set the zero f_{Z1} at 1/4 of the crossover frequency. If R_{COMP} is less than 10KΩ, the equation for C_{COMP} is:

$$C_{COMP1} = \frac{0.637}{R_{COMP} \times fc} (F) \qquad (10)$$

STEP3. If the output capacitor's ESR is high enough to cause a zero at lower than 4 times the crossover frequency, an additional compensation capacitor C_{COMP2} is required. The condition for using C_{COMP2} is:

$$\pi \times C_{OUT} \times R_{ESR} \times fs \geq 1 \qquad (11)$$

And the proper value for C_{COMP2} is:

$$C_{COMP2} = \frac{C_{OUT} R_{ESRCOUT}}{R_{COMP}} \qquad (12)$$

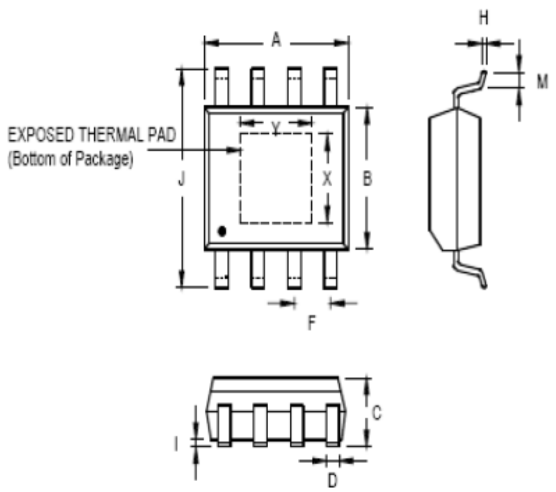
Though C_{COMP2} is unnecessary when the output capacitor has sufficiently low ESR, a small value C_{COMP2} such as 100pF may improve stability against PCB layout parasitic effects

Table 4 — Component Selection Guide for Stability Compensation

Vin Range (V)	Vout (V)	Cout	Rcomp (R3)(kΩ)	Ccomp (C4)(nF)	Ccomp2 (C5)(pF)	Inductor (uH)
5 – 12	1.0	22uFx2 Ceramic	3.3	5.6	none	4.7
5 – 15	1.2		3.9	4.7	none	4.7
5 – 15	1.8		5.6	3.3	none	10
5 – 15	2.5		8.2	2.2	none	10
5 – 15	3.3		10	2	none	10
5 – 15	5		10	3.3	none	10
5 – 12	1.0	470uF/ 6.3V/120mΩ	10	6.8	680	4.7
5 – 15	1.2					
5 – 23	1.8					10
5 – 28	2.5					
5 – 28	3.3					
5 – 28	5					

Package Information

SOP 8L(Exposed PAD) Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.191	0.254	0.008	0.010
I	0.000	0.152	0.000	0.006
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
X	2.057	2.515	0.081	0.099
Y	2.057	3.404	0.081	0.134