2.7V to 30V Input 55μA Quiescent Current Synchronous Boost Controller

EC5086

Description

The EC5086 is a high efficiency synchronous Boost PWM controller that drives all N-channel power MOSFETs to step up output voltage up to 30V. Synchronous rectification increases efficiency, reduces power losses and eases thermal requirements, allowing the EC5086 to be used in high power Step Up applications. The 2.7V to 30V input voltage range supports a wide range of battery and AC powered inputs. The 55μA no load quiescent current extends operating run time in battery-powered systems. The adjustable operating frequency (50kHz to 1MHz) can be synchronized to an external clock with the internal PLL. The EC5086 also features a precision 1.215V reference and a power good output indicator. The SS pin ramps the output voltage during start-up. The MODE/SYNC pin selects between pulse skipping mode and force PWM mode at light loads.

Features

◆30V Maximum Output Voltage
◆2.7V to 30V (40V Abs Max) Input Range
◆Adjustable Input UVLO through EN pin
◆±1% 1.215V Reference Voltage
◆Low Quiescent Current 55μA
◆Shutdown Supply Current 5μA
◆Resistor or Inductor DCR Current Sensing
◆Adjustable Frequency from 50kHz to 1MHz with Synchronization Capability to an external clock
◆Adjustable Output Voltage Soft-Start
◆Output Voltage Power Good Indicator
◆Internal 5.4V LDO for Gate Drive Supply
◆Cycle-by-Cycle Current Limit
◆Thermal Shutdown
◆Pb-Free ROHS compliant
◆QFN3*3mm Packages

Applications

◆Thunderbolt Port for PCs
◆Tablet Computer Accessories
◆5V, 12V, 19V and 24 VDC Bus Power Systems
◆Industrial Battery Powered Systems
◆Power Banks and Electronic Cigarette
◆RF Power Amplifiers
◆Synchronous Flyback

Ordering/Marking Information

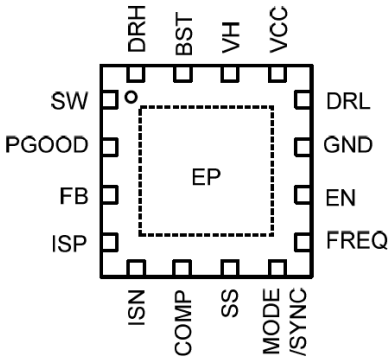
EC5086 NN XX X

R：Tape & Reel

Package Type：
Q1：QFN3*3

Part No.	Marking	Temp. Range	Package	MOQ
EC5086NNQ1R	EC5086 LLLLL YYWW	-40°C ~+85°C	QFN3*3	5,000/Reel

Pin Configurations



EC5086 TOP View

Pin Description

PIN NAME	PIN NO	DESCRIPTION
SW	1	Switching node of the Step-up converter. Connect this pin to the drain of the low sideMOSFET, the source of high side synchronous MOSFET and the inductor.
PGOOD	2	Power Good Indicator. Open-drain output that is pulled to ground when the output voltage is more than ±10% away from the regulated output voltage. A 500kΩ pull-up resistor is recommended between PGOOD and VCC.
FB	3	Error amplifier input and feedback pin for voltage regulation. Connect FB to the center tap of a resistor divider to set the output voltage.
ISP	4	Positive Current Sense Amplifier Input. The current sense resistor is normally placed at the input of the step-up controller in series with the inductor.
ISN	5	Negative Current Sense Amplifier Input. The common mode voltage range on the ISP and ISN pins is 2.5V to 30V (40V abs max).
COMP	6	Output of the internal transconductance error amplifier. The feedback loop compensation network is connected from COMP pin to GND.
SS	7	Soft-start programming pin. A capacitor between the SS pin and AGND pin sets soft-start time.
MODE/SYNC	8	Light Load Pulse-skip mode or Force-PWM mode control and an external clock synchronization input. An internal 100k resistor to GND sets automatically pulse-skip mode at light load condition when the pin is floated. There are three operating modes: · MODE/SYNC low or Float: Operate in pulse-skip mode at light load. · MODE/SYNC high: Operate in force-PWM mode at light load with the oscillator frequency set at FREQ pin by RFREQ. · MODE/SYNC clocked: Operate in force-PWM mode at light load with the oscillator frequency set by SYNC clock input. Force the rising DRL signal to be synchronized with the rising edge of the external clock.
FREQ	9	Oscillator Frequency Set Input. A resistor from FREQ to GND sets the oscillator from 50kHz to 1000kHz (Typical RFREQ=75kΩ sets Fosc=500kHz). RFREQ is still required if an external clock is used at MODE/SYNC pin.
EN	10	Enable input. Pull EN above 1.22V to turn on the converter, and pull EN below 1.11V to shutdown the converter. EN pin can be used to implement adjustable input voltage under voltage lockout (UVLO) using two resistors. Connect EN to the center tap of a resistor divider to set the input UVLO threshold.
GND	11	Ground pin. Connect this pin to the source of the bottom (main) N-channel MOSFET and the (–) terminal(s) of CIN and COUT. All small-signal components and compensation components should also connect to this ground.

DRL	12	Low side gate driver output. Connect this pin to the gate of the low side N-channel MOSFET. When VH bias is removed, an internal 200kΩ resistor pulls DRL to GND.
VCC	13	5.4V On-Chip Low Dropout Linear Regulator Output (LDO). This regulator powers all internal circuitry including the low side and high side N-channel MOSFET gate drivers. Bypass VCC to GND with a 1μF or greater ceramic capacitor.
VH	14	The supply pin to On-Chip LDO Regulator. The operating voltage range on this pin is 2.7V to 30V (40V abs max). Bypass VH to GND with a 0.1μF ceramic capacitor. When the input voltage is below 5.5V, connect VH to the step-up converter output to get maximum 5.4V linear regulator output for gate drivers. When the input voltage is >5.5V, connect VH to the input voltage and improve efficiency.
BST	15	Bootstrap capacitor node for high-side MOSFET gate driver. Connect the bootstrap capacitor 0.1μF from this pin to the SW pin.
DRH	16	High side gate driver output. Connect this pin to the gate of the high side synchronous rectifier N-channel MOSFET.
EP	EP	Exposed pad must be soldered to achieve appropriate power dissipation. Connect EP to GND.

Absolute Maximum Rating (1)

VH, ISP, ISN to GND ..... -0.3V to +40V
Lead Temperature ..... 260°C
ISP to ISN ..... -0.3V to +0.3V
SW to GND ..... -1V to +40V
BST to GND ..... -0.3V to +40V
BST to SW ..... -0.3V to +6V
MODE/SYNC, PGOOD to GND ..... -0.3V to +6V
EN, FB, SS, COMP, VCC to GND ..... -0.3V to +6V
Junction temperature range, TJ ..... -40°C ~+135°C
Storage temperature range, Tstg ..... -55°C~+155°C

Recommend Operating Conditions (2)

Input Voltage (VIN) ..... +2.7V to +30V
Operating Temperature Range ..... -40°C to +85°C
Output Voltage (VOUT) ..... +3V to +30V

Thermal Information (3,4)

Maximum Power Dissipation (TA=+25°C) 1.9W
Thermal Resistance (θJC) QFN3x3-16ld ..... 42.3°C/W
Thermal Resistance (θJA) QFN3x3-16ld ..... 65.7°C/W
Thermal Resistance (ΨJB) QFN3x3-16ld ..... 17.9°C/W

Note(1): Stress exceeding those listed “Absolute Maximum Ratings” may damage the device.
Note(2): The device is not guaranteed to function outside of the recommended operating conditions.
Note(3): Measured on JESD51-7, 4-Layer PCB.
Note(4): The maximum allowable power dissipation is a function of the maximum junction temperature TJ_MAX, the junction to ambient thermal resistance θJA, and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by PD_MAX= (TJ_MAX-TA)/θJA. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

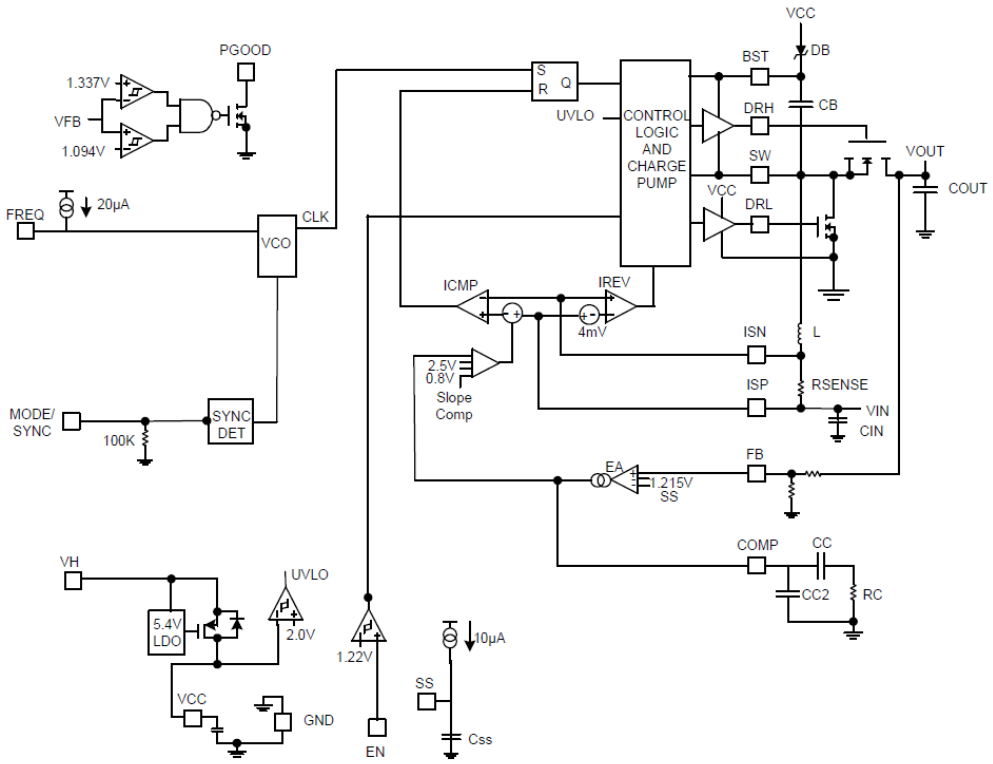
Electrical characteristics

TA = +25°C, 2.7V ≤ VH ≤ 30V, unless otherwise noted. Typical values are at VH=VISP=VISN=12V, VEN=2V and VMODE=0V.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply and Enable					
Input supply range VH		2.7		30	V
Linear Regulator VCC Output Voltage	6V<VH<30V, ICC=1mA	5.18	5.40	5.62	V
	VCC Load Regulation ICC=0mA to 50mA		0.5		%
VCC Under-voltage lockout threshold	VH=VCC Ramp Up VH=VCC Ramp Down		2.0 1.8	2.5	V
EN Pin On Threshold	VEN Rising, Turn On the device	1.12	1.22	1.32	V
EN Pin Off Threshold	VEN Falling, Turn Off the device		1.10		V
EN Pin Input Current	VEN=2V		1		nA
Operating quiescent current into VH	VFB=1.25V, Device no switching		55	80	μA
Shutdown Current	VEN=0.4V		5	10	μA
Error Amplifier and Soft-start					
Feedback voltage VFB		1.203	1.215	1.227	V
Feedback Current IFB	VFB=1.25V		1		nA
Error Amplifier Transconductance	VCOMP=1.2V		2		m mho
COMP pin clamp voltage	Hi Clamp Voltage, VFB=1.1V		2.5		V
	Hi Clamp Voltage, VFB=1.3V		0.8		
Soft-Start Charge Current	VSS=0V	7	10	13	μA
Current Sense Amplifier					
Maximum current sense threshold	ΔV(ISP-ISN)	68	75	82	mV
Reverse current sense threshold	ΔV(ISP-ISN)		4		mV
Current Sense Input Current	VISP=VISN=12V		70		μA
Current Sense Input Range		2.5		30	V
Oscillator and External SYNC Clock					
Oscillator frequency fOSC	RFREQ=60kΩ RFREQ=110kΩ	335	400 800	465	kHz
Maximum Duty Cycle			87		%
Minimum On Time			200		ns
SYNC Input Frequency Range		100		1000	kHz
MODE/SYNC Logic Input Hi		2			V
MODE/SYNC Logic Input Lo				0.4	V
Gate Driver					
Hside Gate Driver DRH On Resistance	DRH high or low		1		Ω
Hside Gate Driver DRL On Resistance	DRL high or low		1		Ω
Power Good Indicator					
PGOOD Low Threshold	VFB with respect to the Feedback Voltage, VFB Falling	87	90	93	%
	Hysteresis, VFB Rising		+3		
PGOOD High Threshold	VFB with respect to the Feedback Voltage, VFB Rising	107	110	113	%
	Hysteresis, VFB Falling		-3		
PGOOD Sink Current	VPGOOD = 0.4V	2	4		mA

PGOOD Leakage Current	VPGOOD = 5V		0.001	1	μA
Thermal Shutdown					
Thermal Shutdown Threshold			160		℃
Thermal Shutdown Hysteresis			35		℃

Functional Block Diagram



Detailed Functional Description

OPEARTION (Refer to the Functional Block Diagram)

The EC5086 is a high-performance wide input range synchronous step-up controllers that accept a 2.7 V to 30 V (40 V abs max) input and support output voltages up to 30V. The devices have gate drivers for both the low side N-channel MOSFET and the high side synchronous rectifier N-channel MOSFET. Voltage regulation is achieved employing constant frequency current mode pulse width modulation (PWM) control. The switching frequency is set either by an external timing resistor or by synchronizing to an external clock signal. The switching frequency is programmable from 100kHz to 1MHz in the resistor programmed mode or can be synchronized to an external clock between 300kHz to 1MHz. The PWM control circuitry turns on the low side MOSFET at the beginning of each oscillator clock cycle, as the error amplifier compares the output voltage feedback signal at the FB pin to the internal 1.215 V reference voltage. The low side MOSFET is turned-off when the inductor current reaches a threshold level set by the error amplifier output. After the low side MOSFET is turned off, the high side synchronous MOSFET is turned on until the beginning of the next oscillator clock cycle or until the inductor current reaches the reverse current sense threshold. The input voltage is applied across the inductor and stores the energy as inductor current ramps up during the portion of the switching cycle when the low side MOSFET is on. Meanwhile the output capacitor supplies load current. When the low side MOSFET is turned off by the PWM controller, the inductor transfers stored energy via the synchronous MOSFET to replenish the output capacitor and supply the load current. This operation repeats every switching cycle. The MODE pin can be used to select different operation modes. Set MODE pin low to enable pulse skip mode and improve efficiency at light load. In pulse skip mode, the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with one or several pulses and goes again into pulse skip mode once the output voltage exceeds the set threshold voltage. This pulse skip mode can be disabled by setting the MODE to VCC. The devices feature internal slope compensation to avoid sub-harmonic oscillation that is intrinsic to peak current mode control at duty cycles higher than 50%. They also feature adjustable soft-start time, optional lossless inductor DCR current sensing, an output power good indicator, cycle-by-cycle current limit and over-temperature protection.

Applications Information

EC5086 can be configured to use either a discrete sense resistor (RSENSE) or inductor DCR (DC resistance) sensing for current sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is becoming popular because it does not require current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. The other external component selection is driven by the load requirement, and begins with the selection of switching frequency, inductor and RSENSE. Next, the power MOSFETs are selected. Finally, input an output capacitors are selected.

Switching Frequency Selections

The first step is to determine the switching frequency of the Step-up converter. There are tradeoffs to consider when selecting a higher or lower switching frequency. Typically, the designer uses the highest switching frequency possible since this results in the smallest solution size. A higher switching frequency allows for lower value inductors and smaller output capacitors compared to a Step-up converter that switches at a lower frequency. A lower switching frequency will produce a larger solution size but typically has a better efficiency by reducing MOSFET switching losses. The switching frequency can also be limited by the minimum on-time of the controller based on the input voltage and the output voltage of the application. Minimum on-time, $t_{ON\,min}$, is the smallest time duration that the EC5086 is capable of turning on the low side MOSFET and correctly sensing inductor current for peak current mode control. The minimum on-time for the EC5086 is approximately 200ns. To determine the maximum allowable switching frequency, first estimate the continuous conduction mode (CCM) duty cycle using Equation 1 with the maximum input voltage.

$$f_{OSCmax} = \frac{D_{min}}{t_{ONmin}} = \frac{\frac{V_{OUT} - V_{INmax}}{V_{OUT}}}{200ns} \qquad \text{(Equation 1)}$$

To determine the timing resistance at FREQ pin for a given switching frequency use the curve in Figure 2.

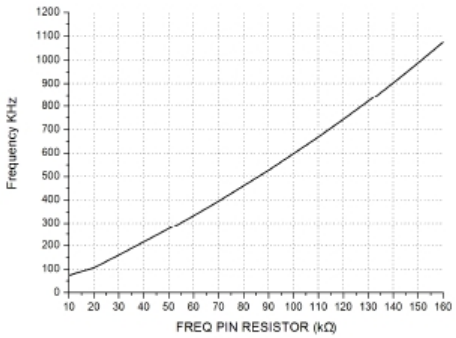


Figure 2. Switching Frequency versus Resistor Value at the FREQ Pin

The EC5086 has an internal phase-locked loop (PLL) comprised of a phase frequency detector, a lowpass filter and a voltage-controlled oscillator (VCO). This allows the turn-on of the low side MOSFET at the rising edge of an external clock signal applied to the MODE/SYNC pin. Typically, the external clock (on MODE/SYNC pin) input logic high threshold is 2 V, while the input logic low threshold is 0.4 V. The EC5086 can only be synchronized to an external clock whose frequency is 100kHz and 1MHz.

Inductor Selection

The selection of the inductor affects the steady-state operation as well as transient behavior and loop stability. These factors make it an important component in a switching power supply design. The three most important inductor specifications to consider are inductor value, DC resistance (DCR), and saturation current rating. In a step-up topology the average inductor current is equal to the input current. The highest average current through the inductor and the switch depends on the maximum output load, converter efficiency η, the minimum input voltage (VINmin), and the output voltage (VOUT). The inductor saturation current rating should be greater (by some margin) than the maximum average inductor average current. Estimation of the maximum average inductor current can be done using Equation 2:

$$I_{Lmax} = I_{OUTmax} \times \frac{V_{OUT}}{V_{INmin} \times \eta} \qquad \text{(Equation 2)}$$

For example, for an output current of 2A at 19V with 85% efficiency, at least 14.9A of average current flows through the inductor at a minimum input voltage of 3V.

The inductor value has a direct effect on ripple current. Let the parameter ΔIL represent the inductor peak-peak ripple current. The inductor ripple current contributes to the output current ripple that must be filtered by the output capacitor. Therefore, choosing high inductor ripple currents impacts the selection of the output capacitor. Higher values of ΔIL lead to discontinuous mode (DCM) operation at moderate to light loads. The inductor ripple current ΔIL decreases with higher inductance or frequency and increases with higher VIN. Estimation of the inductor ripple current can be done using Equation 3:

$$\Delta I_L = \frac{V_{IN}}{f_{OSC} \bullet L}\left(1 - \frac{V_{IN}}{V_{OUT}}\right) \qquad \text{(Equation 3)}$$

Accepting larger values of ΔIL allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is ΔIL = 0.3*ILmax. In a step-up topology, the maximum ripple current ΔIL occurs at 50% duty cycle (VIN = ½*VOUT).

The EC5086 step-up converters have been optimized to operate with an effective inductance in the range of 1μH to 10μH. Larger or smaller inductor values can be used to optimize the performance of the device for specific operating conditions.

ISP and ISN Pins

The ISP and ISN pins are the inputs to the current sense amplifier. The common mode input voltage range of the current sense amplifier is 2.5V to 30V. The current sense resistor is normally placed at the input of the controller in series with the inductor.

The ISP pin also provides power to the current comparator. It draws ~20μA during normal operation. There is a small base current of less than 1μA that flows into the ISN pin. The high impedance ISN input to the current sense amplifier allows accurate DCR sensing.

Filter components mutual to the sense lines should be placed close to the EC5086, and the sense lines should be Kelvin-sense connection underneath the current sense resistor (shown in Figure 3). If DCR sensing is used (Figure 4b), sense resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes.

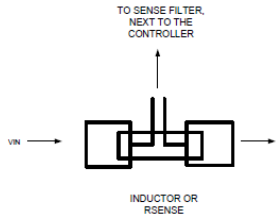
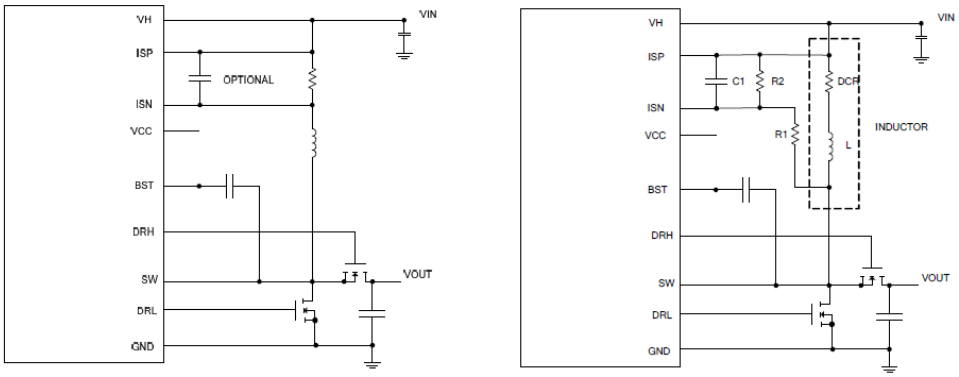


Figure 3. Sense Lines Placement with Inductor or Sense Resistor



(4a) Using a Current Sense Resistor

(4b) Using the Inductor DCR to Sense Current

Figure 4. Two Current Sensing Methods

Current Sensing Resistor

A typical sensing circuit using a discrete resistor is shown in Figure 4a. RSENSE is chosen based on the required maximum average inductor current. The current comparator has a maximum threshold VSENSEmax of 75mV (typical) and 68mV (minimum). To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value

68mV for the maximum current sense threshold VSENSEmax. The current comparator threshold sets the peak of the inductor current, yielding a maximum average inductor current, ILmax, equal to the peak value less half the peak-to-peak ripple current, ΔIL. To calculate the sense resistor value, use the Equation 4:

$$R_{SENSE} = \frac{V_{SENSE\max}}{I_{L\max} + \frac{\Delta I_L}{2}} = \frac{68mV}{I_{L\max} + \frac{\Delta I_L}{2}} \qquad \text{(Equation 4)}$$

Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the EC5086 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 4b. The DCR of the inductor can be less than 1mΩ for high current inductors. In a high current application requiring such an inductor, conduction loss through a sense resistor could reduce the efficiency by a few percent compared to DCR sensing.

If the external R1||R2 • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature. Consult the manufacturer's data sheets for detailed information. Using the inductor ripple current value from the inductor section, the target sense resistor value is calculated with Equation 5:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE\max}}{I_{L\max} + \frac{\Delta I_L}{2}} = \frac{68mV}{I_{L\max} + \frac{\Delta I_L}{2}} \qquad \text{(Equation 5)}$$

C1 is usually selected to be in the range of 0.1μF to 0.47μF. This forces R1|| R2 to around 2kΩ, reducing error that might have been caused by the ISN pin ±1μA current.

Power MOSFET Selection

Two external power MOSFETs must be selected for the EC5086: one N-channel MOSFET for the low side (main) switch, and one N-channel MOSFET for the high side (synchronous) switch. The maximum gate drive voltage levels are set by the VCC voltage which is typically 5.4V. Consequently, use logic-level threshold MOSFETs in most applications. Two primary considerations when selecting the power MOSFETs are the average gate drive current required and the estimated MOSFET power losses. The average gate drive current must be less than the 50mA (minimum) VCC supply current limit. This current is calculated using Equation 6. With the selected power block and 5.4V VCC, the low-side FET has a total gate charge of 10nC and the high-side FET has a total gate charge of 5nC. The required gate drive current is 12mA for 800kHz switching frequency.

$$I_{GateDriver} = (Q_{gHS} + Q_{gLS}) \times f_{OSC} = (5nC + 10nC) \times 800kHz = 12mA \qquad \text{(Equation 6)}$$

The two largest components of power loss in the MOSFETs are switching and conduction losses. Both losses are the highest at the minimum input voltage when the output current is the maximum.

Input Capacitor Selection

Place a high quality 0.1μF in parallel with at least a 10μF or higher ceramic type X5R or X7R bypass capacitor at the VIN pin to power ground PGND for proper decoupling. Based on the application requirements additional bulk capacitance are needed to meet input voltage ripple, transient and EMI requirements. The value of the CIN is a function of the source impedance, and in general, the higher the source impedance, the higher the required input capacitance. The required amount of input capacitance is also greatly affected by the duty cycle. High output current applications that also experience high duty cycles can place great demands on the input supply, both in terms of DC current and ripple current. The input capacitor voltage rating should comfortably exceed the maximum input voltage.

Setting Input Under-voltage Lockout (UVLO)

The EN pin voltage must be greater than 1.22 V (typical) to enable EC5086. The device enters shutdown mode when the EN voltage is less than 0.4V. In shutdown mode, the input supply current for the device is less than 5μA. When the EN pin voltage is higher than the shutdown threshold but less than 1.22V, the devices are in standby mode. Adjustable input UVLO can be accomplished using the EN pin. As shown in Figure 5, a resistor divider from the VIN pin to GND sets the input UVLO level.

Choose the bottom UVLO resistor RUVLO_BOT in the 10kΩ~200kΩ range to set the divider current at 10μA or higher. Typically select RUVLO_BOT=100kΩ. The value of top resistor RUVLO_TOP, depending on the the desired turn-on voltage VSTART at the VIN pin, can be calculated with Equation 7:

$$R_{UVLO\_TOP} = R_{UVLO\_BOT} \times \left(\frac{V_{START}}{V_{EN}} - 1 \right) = 100k\Omega \times \left(\frac{V_{START}}{1.22V} - 1 \right) \quad \text{(Equation 7)}$$

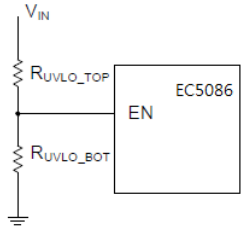


Figure 5. Input UVLO Setting

Connect EN pin to VCC pin if input UVLO function is not used.

Output Capacitor Selection

In a step-up converter, the output has a discontinuous current, so output capacitor COUT must be capable of reducing the output voltage ripple and filtering the high di/dt path of the supply. It is recommended to use X5R or X7R ceramic capacitors placed as close as possible to the VOUT pin and power ground PGND pin. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The steady ripple voltage due to charging and discharging the bulk output capacitance in a single phase step-up converter is given by Equation 8. This value does not take into account the ESR of the output capacitor.

$$\Delta V_{OUT} = \frac{I_{OUT\,max} \times D_{max}}{C_{OUT} \times f_{OSC}} = \frac{I_{OUT\,max} \times \frac{V_{OUT} - V_{IN\,min}}{V_{OUT}}}{C_{OUT} \times f_{OSC}} \quad \text{(Equation 8)}$$

where COUT is the output filter capacitor.

For example: Build 5V nominal output voltage from the minimum 3V input supply voltage. Select switching frequency 600kHz. Choose output capacitor to get less than 50mV ripple (1% of VOUT) at maximum 4Amp output current. The minimum output capacitor is 53μF required to limit the output voltage ripple.

$$C_{OUT} \geq \frac{I_{OUT\,max} \times D_{max}}{\Delta V_{OUT} \times f_{OSC}} = \frac{4A \times \frac{5V - 3V}{5V}}{5V \times 1\% \times 600kHz} = 53\mu F$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Ceramic capacitors have excellent low ESR characteristics but can have a DC Bias effect, which will have a strong influence on the final effective capacitance. Capacitance deratings for aging, temperature and dc bias increase the minimum value required. The voltage rating must be greater than the output voltage with some tolerance for output voltage ripple and overshoot in transient conditions. For this example 4 x 22μF, 25 V ceramic capacitors with 5 mΩ of ESR are used. The 40% derated capacitance is 52.8μF, approximately equal to the calculated minimum.

Setting Output Voltage

The EC5086 output voltage is set by an external feedback resistor divider carefully placed across the output, as shown in Figure 6. Great care should be taken to route the VFB line away from noise sources, such as the inductor or the SW line. Also, keep the FB trace as short as possible to avoid noise pickup. The typical value of the voltage on the FB pin is 1.215V. The maximum allowed value for the output voltage is 30V. Choose the bottom resistor RFB_BOT in the 10kΩ~200kΩ range to set the divider current at 6μA or higher. Typically select RFB_BOT=100kΩ. The value of top resistor RFB_TOP, depending on the needed output voltage VOUT, can be calculated using Equation 8:

$$R_{FB\_TOP} = R_{FB\_BOT} \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) = 100k\Omega \times \left(\frac{V_{OUT}}{1.215V} - 1 \right) \quad \text{(Equation 8)}$$

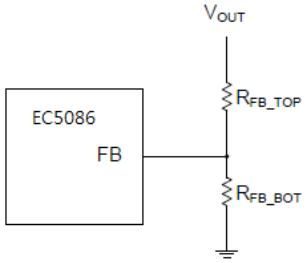


Figure 6. Output Voltage Setting

Soft-Start (SS Pin)

The VOUT start-up time is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the internal 1.215V
reference, the EC5086 regulates the VFB pin voltage to the voltage on the SS pin instead of 1.215V. Soft-start is enabled by simply connecting a capacitor from the SS pin to ground, as shown in Figure 7. An internal 10μA current source charges the capacitor, providing a linear ramping voltage at the SS pin. The EC5086 will regulate the VFB and VOUT voltage smoothly from VIN to its final regulated value according to the voltage on the SS pin. The total soft-start time will be approximately calculated with
Equation 9:

$$t_{SS} = C_{SS} \bullet \frac{1.215V}{10\mu A} \qquad \text{(Equation 9)}$$

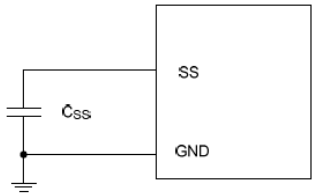


Figure 7. Using the SS Pin to Program Soft-Start

Bootstrap Capacitor Selection

Place a 0.1μF~1μF X5R or X7R ceramic capacitor between the BST and SW pins for proper operation. This capacitor provides the instantaneous charge and gate drive voltage needed to turn on the high-side MOSFET.

VCC Low-Dropout Linear Regulator

The EC5086 features an internal P-channel low dropout linear regulator (LDO) that supplies power to the VCC pin from the VIN supply pin. VCC powers the gate drivers and much of the EC5086's internal circuitry. The LDO output VCC is regulated to 5.4V. It can supply at least 50mA and must be bypassed to ground with a minimum of 1μF X5R or better grade ceramic capacitor. The capacitor should have a 10 V or higher voltage rating.Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers. A VCC under-voltage detection circuit prevents the internal PWM control circuitry and gate drivers from operation when VCC voltage is below 2V (typical).

Power Good

The PGOOD pin is connected to an open-drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the VFB pin voltage is not within ±10% of the 1.215V reference voltage. The PGOOD pin is also pulled low when the corresponding EN pin is low (shut down). When the FB pin voltage is within the ±10% regulation threshold range, the internal MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to VCC pin.

The Control Loop Compensation

The series RC-CC filter at COMP pin sets the dominant pole-zero loop compensation. The resistor RC in series with a capacitor CC creates a compensating zero. A capacitor CC2 in parallel to these two components can be added to form a compensating pole. In a step-up topology, the maximum crossover frequency is typically limited by the right-half plane zero (RHPZ). The compensation design should be done at the minimum input voltage and full load when the RHPZ is at the lowest frequency. The crossover frequency should also be limited to less than 1/4 of the RHPZ frequency.

Table 1. Gives RC, CC and CC2 values for certain inductors, input and output voltages providing a very stable system. For a faster
response time, a higher RC value can be used to enlarge the bandwidth, as well as a slightly lower value of CC to keep enough phase margin. These adjustments should be performed in parallel with the load transient response monitoring of EC5086.

Table 1. Recommended Compensation Network Values

Application	I_{OUT_MAX}	Frequency	Inductor	R_{SENSE}	C_{IN}	C_{OUT}	R_C	C_C and C_{C2}
1-Cell step-up to 5V Vin Range: 3V~4.35V	4A	600kHz	1.5μH I_{SAT}=8A	8mΩ	3*22μF 16V	4*22μF 16V	1kΩ	C_C=22nF C_{C2}=open
1-Cell step-up to 12V Vin Range: 3V~4.35V	2A	800kHz	3.3μH I_{SAT}=10A	6mΩ	3*22μF 25V	4*22μF 25V	10kΩ	C_C=22nF C_{C2}=open

Layout consideration

Use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for analog ground to minimize the effects of ground noise. Connect these ground nodes at any place close to the ground pins of the IC.

Thermal information

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component. Three basic approaches for enhancing thermal performance are listed below: Improve the power dissipation capability of the PCB design Improve the thermal coupling of the component to the PCB Introducing airflow in the system

The maximum junction temperature (TJ) of the EC5086 devices is 150℃.The thermal resistance of the 16-pin QFN package is RJA = 45℃/W, if the Exposed PAD is soldered. Specified regulator operation is assured to a maximum ambient temperature TA of +85℃. Therefore, the maximum power dissipation for the 16-pin QFN package it is about 0.99W. More power can be dissipated if the maximum ambient temperature of the application is lower.

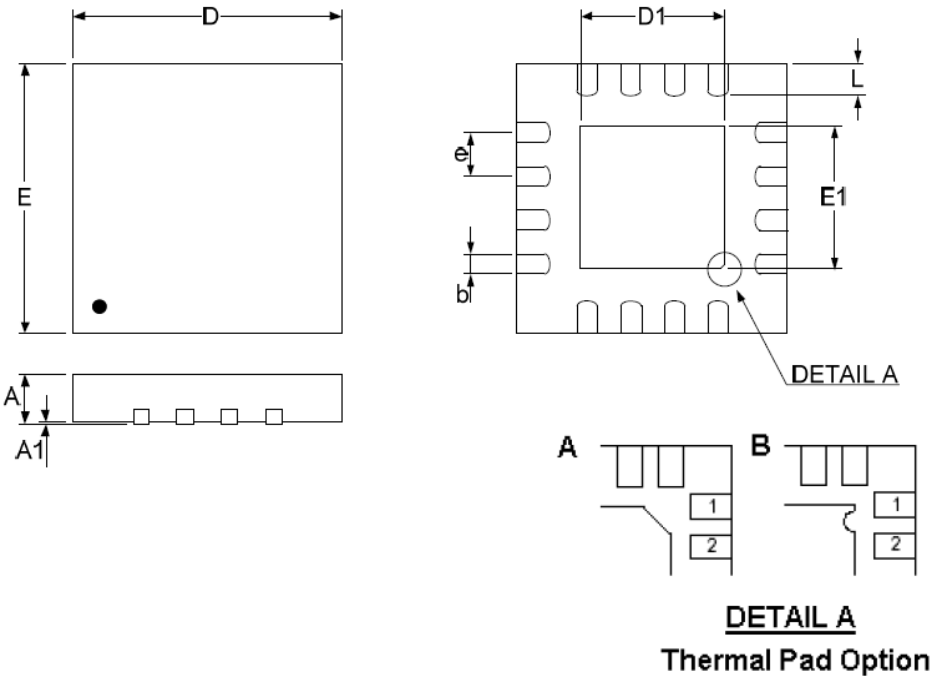
$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{150℃\text{-}85℃}{65.7℃/W} = 0.99W$$

The EC5086 internal P-channel low dropout linear regulator (LDO) can supply 50mA current at the VCC pin from the VH supply pin. VCC powers the gate drivers and much of the EC5086's internal circuitry. High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the EC5086 to be exceeded. The power dissipation for the IC is equal to (VIN-VCC)* IVCC. The gate charge current is dependent on operating frequency. The junction temperature can be estimated by package thermal resistance θJA. For example, at +85°C ambient temperature, the EC5086 VCC current is limited to less than 40mA in the QFN package from a 30V supply:

TJ= 85°C + (40mA)(30V-5.4V)(65.7°C/W) = 150°C

Packaging Information

QFN3*3



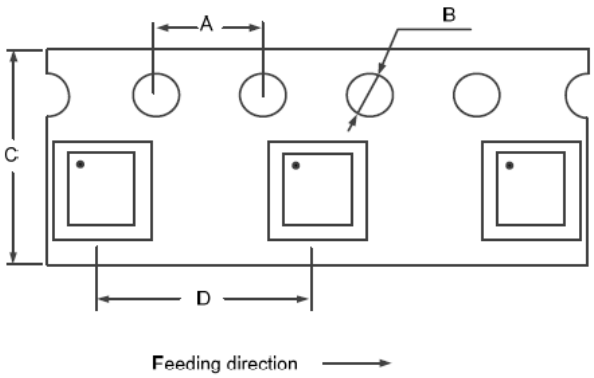
DETAIL A

Thermal Pad Option

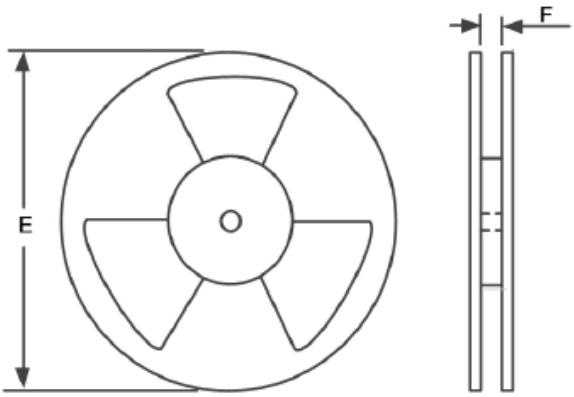
SYMBOLS	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.18	0.30	0.007	0.012
E	2.90	3.10	0.114	0.122
D	2.90	3.10	0.114	0.122
D1	1.70		0.067	
E1	1.70		0.067	
e	0.50		0.020	
L	0.30	0.50	0.012	0.020

Carrier Tape & Reel Dimensions

1.Orientation / Carrier Tape Information :



2.Rokreel Information :



3.Dimension Details :

PKG Type	A	B	C	D	E	F	Q'ty/Reel
Q(D)FN 3x3	4.0 mm	1.5 mm	12.0 mm	8.0 mm	13 inches	13.0 mm	5,000

Reflow Profile

Classification Of IR Reflow Profile

Reflow Profile	Green Assembly
Average Ramp-Up Rate (Tsmin to Tp)	1~2℃/second, 3℃/second max.
Preheat & Soak -Temperature Min(Tsmin) -Temperature Max(Tsmax) -Time(tsmin to ts tsmax)	150℃ 200℃ 60~120 seconds
Time maintained above: -Temperature(TL) -Time(tL)	217℃ 60~150 seconds
Peak Temperature(Tp)	See Classification Temp in table 1
Time within 5℃ of actual Peak Temperature(tp)	30 seconds max.
Ramp-Down Rate	6℃/second max.
Time 25℃ to Peak Temperature	8 minutes max.

* Tolerance for peak profile Temperature (Tp) is defined as a supplier minimum and a user maximum.
** Tolerance for time at peak profile temperature (tp) is defined as a supplier minimum and a user maximum.

Table 1. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm³ <350	Volume mm³ 350-2000	Volume mm³ >2000
<1.6 mm	260 ℃	260 ℃	260 ℃
1.6 mm – 2.5 mm	260 ℃	250 ℃	245 ℃
≥2.5 mm	250 ℃	245 ℃	245 ℃

Note: For all temperature information, please refer to topside of the package, measured on the package body surface.