General Description

The EC5732 amplifier is Dual supply, micro-power, zero-drift CMOS operational amplifier, the amplifier offer bandwidth of 350kHz, rail-to-rail inputs and outputs, and single-supply operation from 2.5V to 5.5V. EC5732 uses chopper stabilized technique to provide very low offset voltage (less than 20µV maximum) and near zero drift over temperature. Low quiescent supply current of 20µA and very low input bias current of 10pA make the devices an ideal choice for low offset, low power consumption and high impedance applications. The EC5732 is available in SOP-8L and MOSP-8L packages. The extended temperature range of -40℃ to +125℃ over all supply voltages offers additional design flexibility.

Features

- Single-Supply Operation from +2.5V ~ +5.5V
- Rail-to-Rail Input / Output
- Gain-Bandwidth Product: 350kHz (Typ.)
- Quiescent Current per Amplifier: 20µA (Typ.)
- Zero Drift：0.05uV/℃(Max.)
- Low offset voltage：20uV(Max.@25℃)
- Low input Bias Current：10pA(Typ.@25℃)
- Slew Rate：0.1V/us(Typ.)
- Total Hamonic Distortion plus Noise：0.005%(Typ.)
- Embedded RF Anti-EMI filter.
- Operating Temperature: -40°C ~ +125°C
- Available in SOP-8L and MSOP-8L Packages

Applications

- Portable Equipment
- Mobile Communications
- Filter and Buffer
- Sensor Interface
- Medical Instrumentation
- Battery-Powered Instruments
- Handheld Test Equipment

Pin Assignments

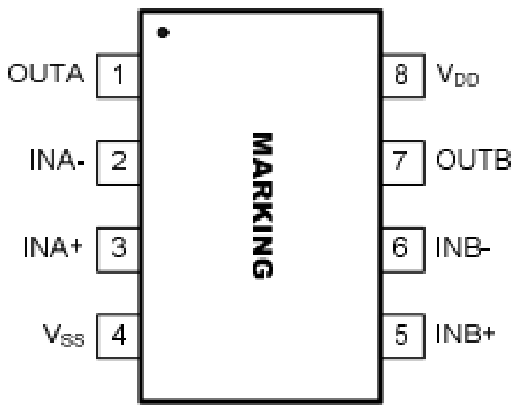
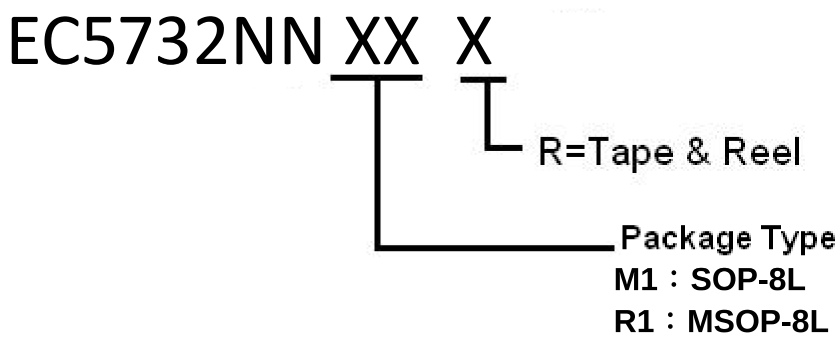


Figure 1. Pin Assignment Diagram (SOP-8L and MSOP-8L Package)

Ordering Information



Part Number	Package	Marking	Marking Information
EC5732NNM1R	SOP-8L	EC5732 LLLLL YYWWT	1. LLLLL：Last five Number of Lot No 2. YY：Year Code 3. WW：Week Code 4. T：Internal Tracking Code
EC5732NNR1R	MSOP-8L	5732 LLLL YYWW	1. LLLL：Last four Number of Lot No 2. YY：Year Code 3. WW：Week Code

Electrical Characteristics

Absolute Maximum Ratings

Condition	Min	Max
Power Supply Voltage (V_{DD} to Vss)	-0.5V	+7V
Analog Input Voltage (IN+ or IN-)	Vss-0.5V	V_{DD}+0.5V
PDB Input Voltage	Vss-0.5V	+7V
Operating Temperature Range	-40°C	+125°C
Junction Temperature	+150°C	
Storage Temperature Range	-65°C	+150°C
Lead Temperature (soldering, 10sec)	+300°C	
Package Thermal Resistance (T_A=+25°C)		
SOP-8L, θ_{JA}	130°C	
MSOP-8L, θ_{JA}	210°C	

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

(V_{DD} = +5V, Vss = 0V, V_{CM} = 0V, V_{OUT} = V_{DD}/2, RL=10K tied to V_{DD}/2, SHDNB = V_{DD}, TA = -40°C to +125°C, unless otherwise noted. Typical values are at T_A =+25°C.) (Notes 1)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Supply-Voltage Range	V_{DD}	Guaranteed by the PSRR test	2.5	-	5.5	V
Quiescent Supply Current (per Amplifier)	I_Q	V_{DD} = 5V	14	20	26	μA
Input Offset Voltage	V_{OS}		-	-	±20	μV
Input Offset Voltage Tempco	$\Delta V_{OS}/\Delta T$		-	-	0.05	μV/°C
Input Bias Current	I_B	(Note 2)	-	10	-	pA
Input Offset Current	I_{OS}	(Note 2)	-	100	-	pA
Input Common-Mode Voltage Range	V_{CM}		-0.1	-	V_{DD}+0.1	V
Common-Mode Rejection Ratio	CMRR	V_{DD}=5.5 Vss-0.1V≤V_{CM}≤V_{DD}+0.1V	90	110	-	dB
		Vss≤V_{CM}≤5V	95	115	-	dB
Power-Supply Rejection Ratio	PSRR	V_{DD} = +2.5V to +5.5V	85	105	-	dB
Open-Loop Voltage Gain	A_V	V_{DD}=5V, R_L=10kΩ, 0.05V≤V_O≤4.95V	100	120	-	dB

Electrical Characteristics(Continued)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Voltage Swing	V_{OUT}	$\|V_{IN+}-V_{IN-}\| \geq 10mV$, $R_L = 100k\Omega$ to $V_{DD}/2$, $V_{DD}-V_{OH}$	-	6	-	mV
		$\|V_{IN+}-V_{IN-}\| \geq 10mV$, $R_L = 100k\Omega$ to $V_{DD}/2$, $V_{OL}-V_{SS}$	-	6	-	mV
		$\|V_{IN+}-V_{IN-}\| \geq 10mV$, $R_L = 5k\Omega$ to $V_{DD}/2$, $V_{DD}-V_{OH}$	-	60	-	mV
		$\|V_{IN+}-V_{IN-}\| \geq 10mV$, $R_L = 5k\Omega$ to $V_{DD}/2$, $V_{OL}-V_{SS}$	-	60	-	mV
Output Short-Circuit Current	I_{SC}	Sinking or Sourcing	-	±5	-	mA
Gain Bandwidth Product	GBW	A_V = +1V/V	-	350	-	kHz
Slew Rate	SR	A_V = +1V/V	-	0.1	-	V/μs
Settling Time	t_S	To 0.1%, V_{OUT} = 2V step A_V = +1V/V	-	20	-	μs
Over Load Recovery Time		$V_{IN} \times$ Gain=V_S	-	100	-	μs
Input Voltage Noise Density	e_n	f = 1kHz	-	70	-	nV/√Hz
		f = 10kHz	-	60	-	
Total Harmonic Distortion plus Noise	THD+N	V_{OUT} = 2V_{PP},A_V = +1V/V, R_L = 10kΩ to GND, f = 1kHz	-	0.005	-	%
		V_{OUT} = 2V_{PP},A_V = +1V/V, R_L =10kΩ to GND, f = 10kHz	-	0.1	-	

Note 1: All devices are 100% production tested at T_A = +25°C; all specifications over the automotive temperature range is guaranteed by design, not production tested.

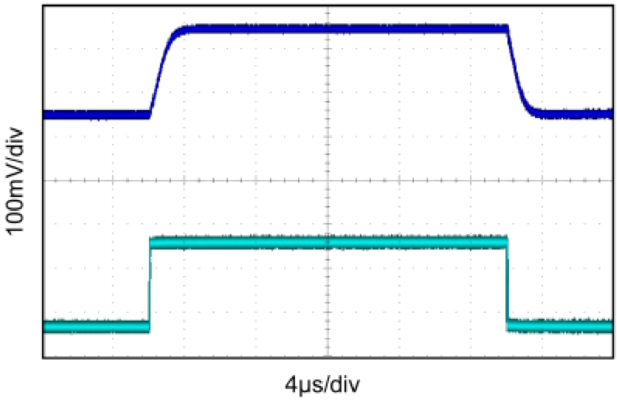
Note 2: Parameter is guaranteed by design.

Typical characteristics

At T_A=+25°C, RL=10 kΩ connected to $V_S/2$ and V_{OUT}= $V_S/2$, unless otherwise noted.

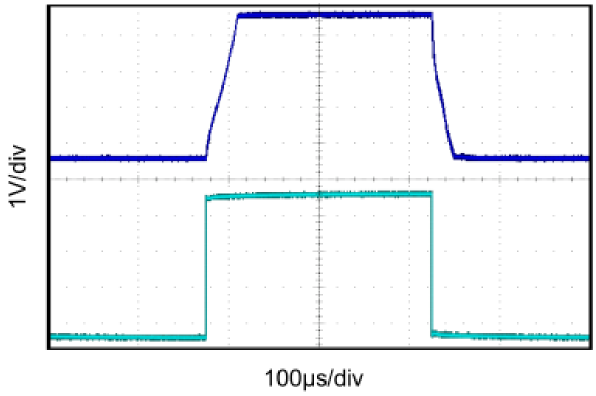
Small Signal Step Response

G=+1V/V,RL=10kΩ,CL=0pF

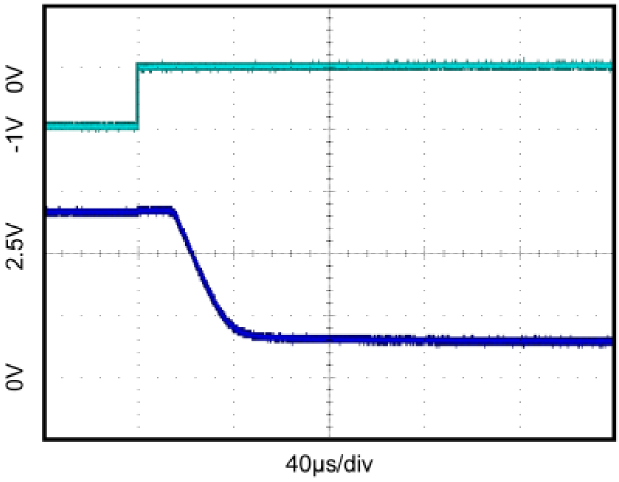


Large Signal Step Response

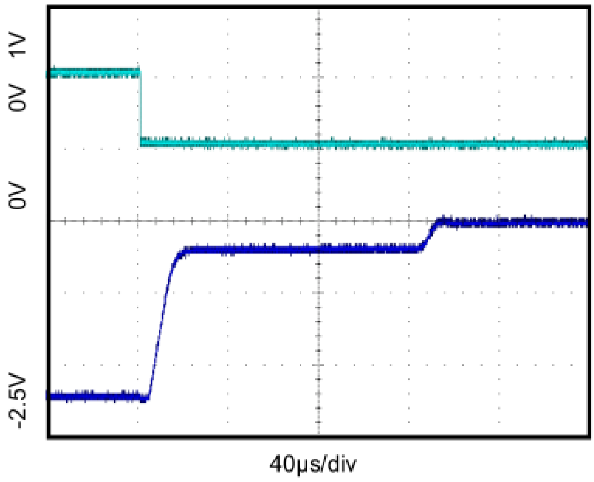
G=+1V/V,RL=100kΩ,CL=100pF



Positive Over-Voltage Recovery

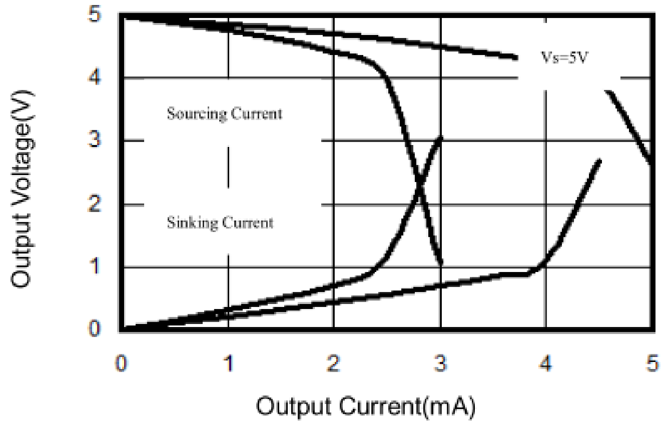


Negative Over-Voltage Recovery

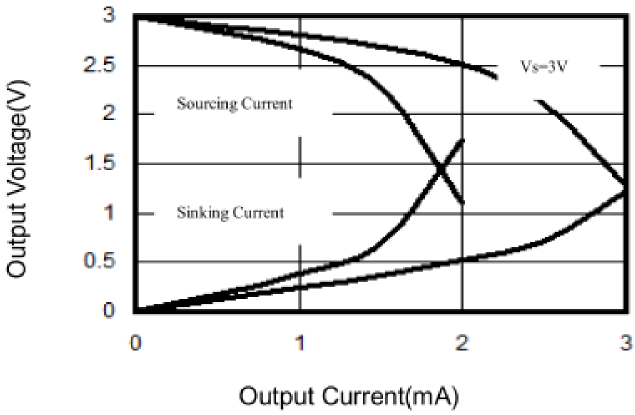


Typical characteristics(Continued)

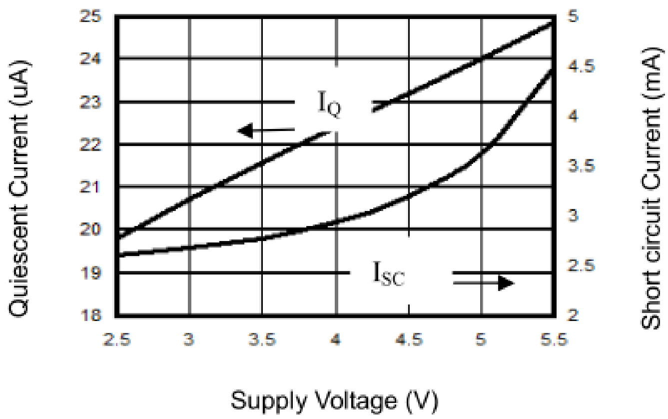
Output Voltage Swing vs. Output Current



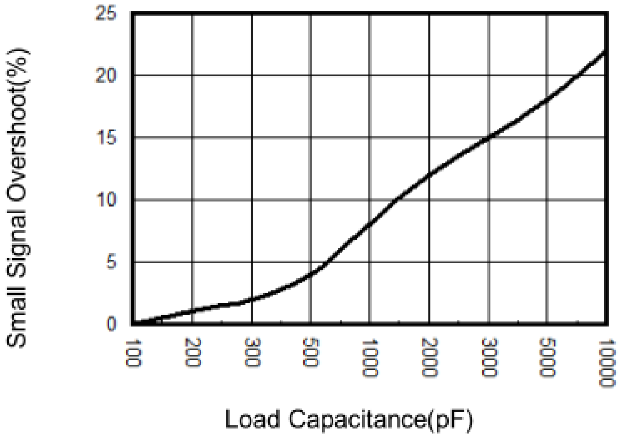
Output Voltage Swing vs. Output Current



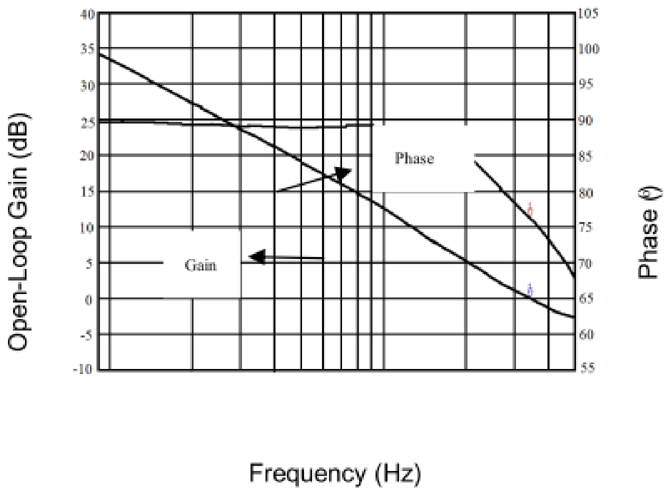
Quiescent and Short-Circuit Current vs. Supply Voltage



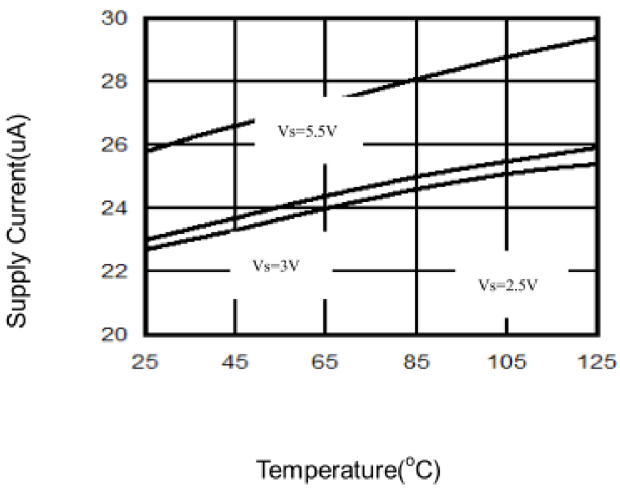
Small Signal Overshoot vs. Load Capacitance



Open-Loop Gain And Phase vs. Frequency



Supply Current vs. Temperature



Application Information

Size

EC5732 series op amps are unity-gain stable and suitable for a wide range of general-purpose applications. The small footprints of the EC5732 series packages save space on printed circuit boards and enable the design of smaller electronic products.

Power Supply Bypassing and Board Layout

EC5732 series operates from a single 2.5V to 5.5V supply or dual ±1.25V to ±2.75V supplies. For best performance, a 0.1µF ceramic capacitor should be placed close to the V_{DD} pin in single supply operation. For dual supply operation, both V_{DD} and V_{SS} supplies should be bypassed to ground with separate 0.1µF ceramic capacitors.

Low Supply Current

The low supply current (typical 40µA) of EC5732 series will help to maximize battery life. They are ideal for battery powered systems

Operating Voltage

EC5732 series operate under wide input supply voltage (2.5V to 5.5V). In addition, all temperature specifications apply from -40℃ to +125℃. Most behavior remains unchanged throughout the full operating voltage range. These guarantees ensure operation throughout the single Li-Ion battery lifetime

Rail-to-Rail Input

The input common-mode range of EC5732 series extends 100mV beyond the supply rails (V_{SS}-0.1V to V_{DD}+0.1V). This is achieved by using complementary input stage. For normal operation, inputs should be limited to this range.

Rail-to-Rail Output

Rail-to-Rail output swing provides maximum possible dynamic range at the output. This is particularly important when operating in low supply voltages. The output voltage of EC5732series can typically swing to less than 10mV from supply rail in light resistive loads (>100kΩ), and 60mV of supply rail in moderate resistive loads (5kΩ).

Capacitive Load Tolerance

The EC5732 series can directly drive 250pF capacitive load in unity-gain without oscillation. Increasing the gain enhances the amplifier's ability to drive greater capacitive loads. In unity-gain configurations, the capacitive load drive can be improved by inserting an isolation resistor R_{ISO} in series with the capacitive load, as shown in Figure 2.

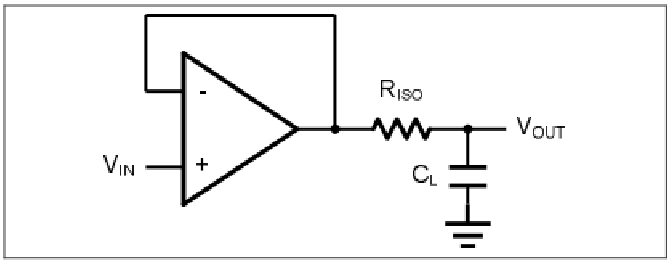


Figure 2. Indirectly Driving a Capacitive Load Using Isolation Resistor

The bigger the R_{ISO} resistor value, the more stable V_{OUT} will be. However, if there is a resistive load RL in parallel with the capacitive load, a voltage divider (proportional to R_{ISO}/R_L) is formed, this will result in a gain error.
The circuit in Figure 3 is an improvement to the one in Figure 2. RF provides the DC accuracy by feed-forward the V_{IN} to R_L. C_F and R_{ISO} serve to counteract the loss of phase margin by feeding the high frequency component of the output signal back to the amplifier's inverting input, thereby preserving the phase margin in the overall feedback loop. Capacitive drive can be increased by increasing the value of C_F. This in turn will slow down the pulse response.

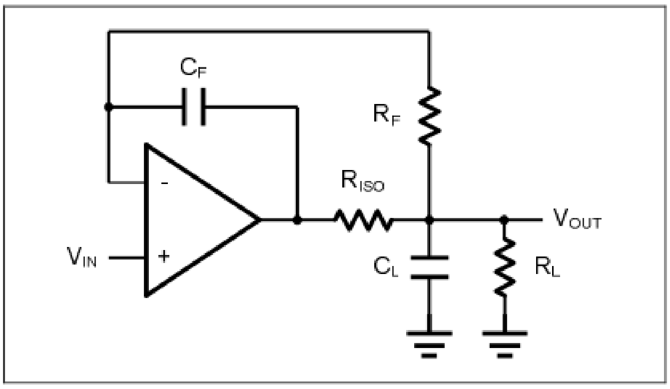


Figure 3. Indirectly Driving a Capacitive Load with DC Accuracy

Differential amplifier

The differential amplifier allows the subtraction of two input voltages or cancellation of a signal common the two inputs. It is useful as a computational amplifier in making adifferential to single-end conversion or in rejecting a common mode signal. Figure 4. shown the differential amplifier using EC5732.

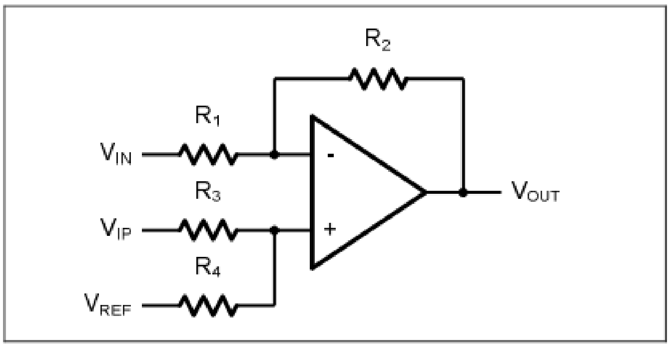


Figure 4. Differential Amplifier

$$V_{OUT}=\left(\frac{R1+R2}{R3+R4}\right)\frac{R4}{R1}V_{IN}-\frac{R2}{R1}V_{IP}+\left(\frac{R1+R2}{R3+R4}\right)\frac{R3}{R1}V_{REF}$$

If the resistor ratios are equal (i.e. R_1=R_3 and R_2=R_4), then

$$V_{OUT}=\frac{R2}{R1}(V_{IP}-V_{IN})+V_{REF}$$

Instrumentation Amplifier

The input impedance of the previous differential amplifier is set by the resistors R1, R2, R3, and R4. To maintain the high input impedance, one can use a voltage follower infront of each input as shown in the following two instrumentation amplifiers.

Three-Op-Amp Instrumentation Amplifier

The dual EC5732 can be used to build a three-op-amp instrumentation amplifier as shown in Figure 5.

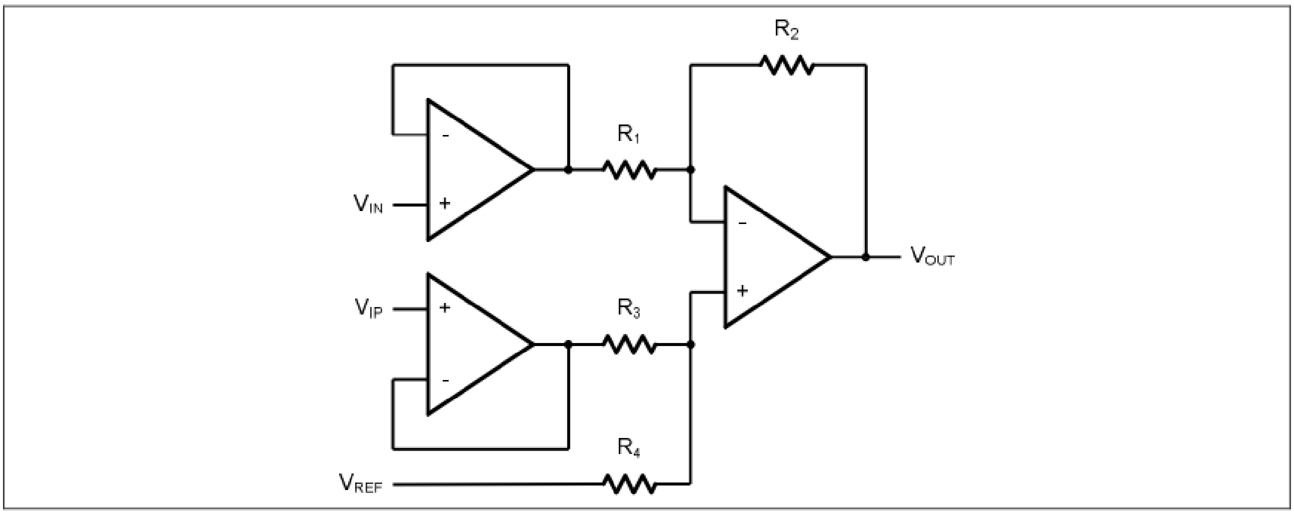


Figure 5. Three-Op-Amp Instrumentation Amplifier

The amplifier in Figure 5 is a high input impedance differential amplifier with gain of R2/R1. The two differential voltage followers assure the high input impedance of the amplifier.

$$V_{OUT} = (1 + \frac{R4}{R3})(V_{IP} - V_{IN})$$

Two-Op-Amp Instrumentation Amplifier

EC5732 can also be used to make a high input impedance two-op-amp instrumentation amplifier as shown in Figure 6.

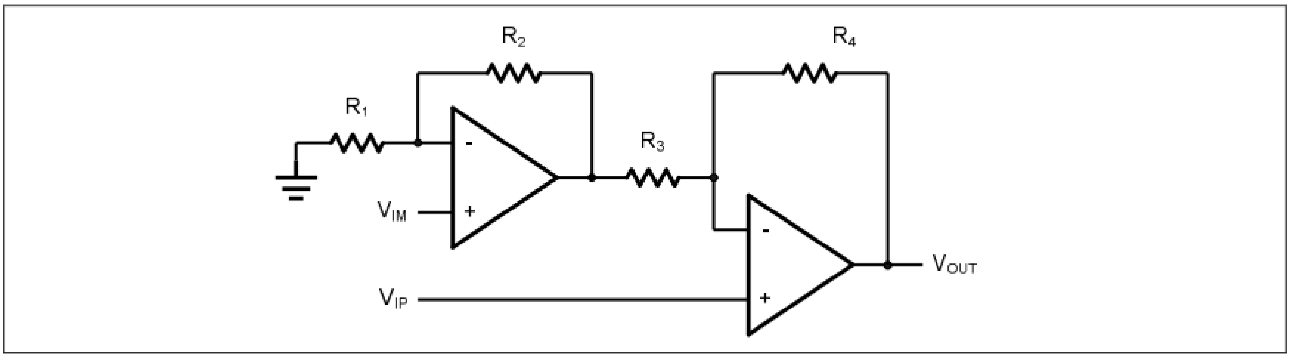


Figure 6. Two-Op-Amp Instrumentation Amplifier

Where $R_1=R_3$ and $R_2=R_4$. If all resistors are equal, then $V_{OUT}=2(V_{IP}-V_{IN})$

Single-Supply Inverting Amplifier

The inverting amplifier is shown in Figure 7. The capacitor C1 is used to block the DC signal going into the

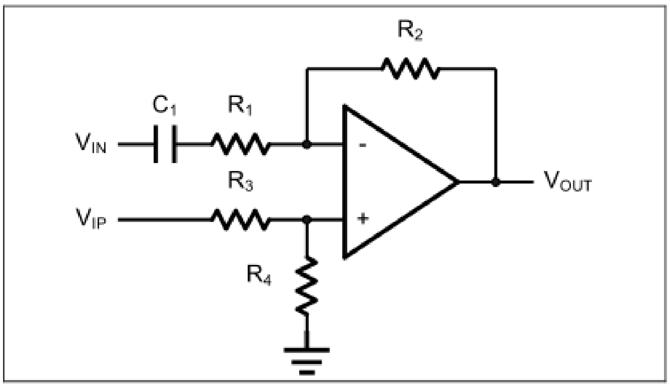


Figure 7. Single Supply Inverting Amplifier

Low Pass Active Filter

The low pass active filter is shown in Figure 8. The DC gain is defined by $-R_2/R_1$. The filter has a -20dB/decade roll-off after its corner frequency $f_C=1/(2\pi R_3C_1)$.

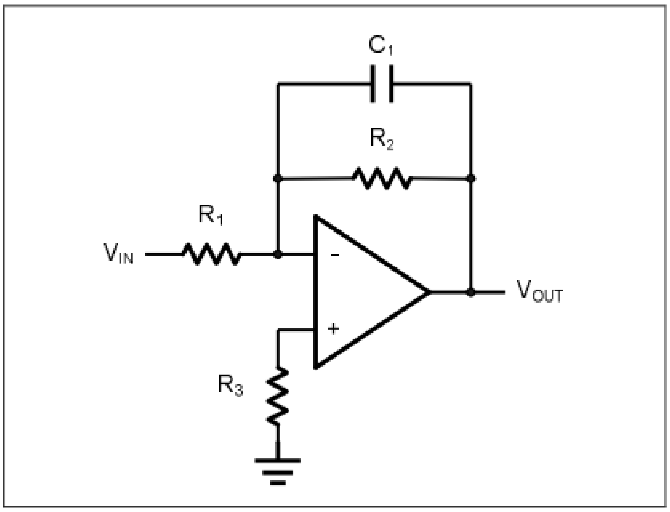


Figure 8. Low Pass Active Filter

Sallen-Key 2nd Order Active Low-Pass Filter

EC5732 can be used to form a 2nd order Sallen-Key active low-pass filter as shown in Figure 9. The transfer function from VIN to V_{OUT} is given by

$$\frac{V_{OUT}}{V_{IN}}(S)=\frac{\frac{1}{C_1C_2R_1R_2}A_{LP}}{S^2+S\left(\frac{1}{C_1R_1}+\frac{1}{C_1R_2}+\frac{1}{C_2R_2}-\frac{A_{LP}}{C_2R_2}\right)+\frac{1}{C_1C_2R_1R_2}}$$

Where the DC gain is defined by $A_{LP}=1+R_3/R_4$, and the corner frequency is given by AC signal source VIN. The value of R_1 and C_1 set the cut-off frequency to $f_C=1/(2\pi R_1C_1)$. The DC gain is defined by $V_{OUT}=-(R_2/R_1)V_{IN}$

$$\omega C=\sqrt{\frac{1}{C_1C_2R_1R_2}}$$

The pole quality factor is given by

$$\frac{\omega C}{Q}=\frac{1}{C_1R_1}+\frac{1}{C_1R_2}+\frac{1}{C_2R_2}-\frac{A_{LP}}{C_2R_2}$$

Let R1=R2=R and C1=C2=C, the corner frequency and the pole quality factor can be simplified as below

$$\omega_C = \frac{1}{CR}$$

And $Q=2-R_3/R_4$

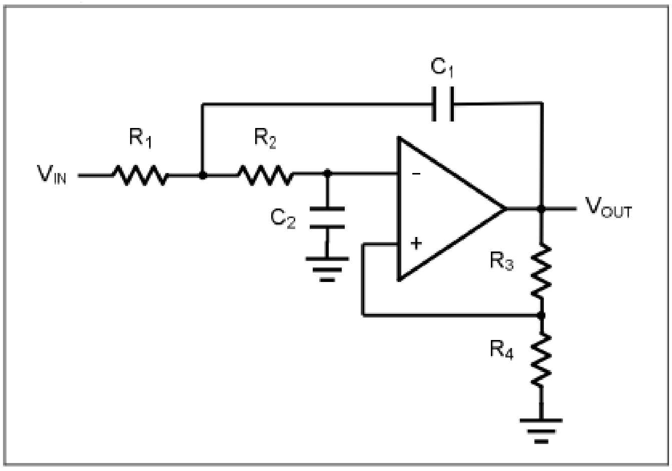
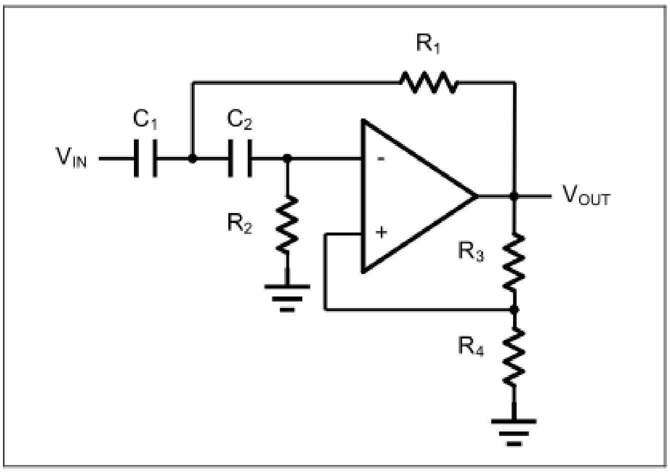


Figure 9. Sanllen-Key 2nd Order Active Low-Pass Filter

Sallen-Key 2nd Order high-Pass Active Filter

The 2nd order Sallen-key high-pass filter can be built by simply interchanging those frequency selective components R_1, R_2, C_1, and C_2 as shown in Figure 10.



$$\frac{V_{OUT}}{V_{IN}}(S) = \frac{S^2 A_{HP}}{S^2 + S\left(\frac{1}{C_1R_1} + \frac{1}{C_2R_2} + \frac{1-A_{HP}}{C_1R_1}\right) + \frac{1}{C_1C_2R_1R_2}}$$

Where $A_{HP}=1+R_3/R_4$

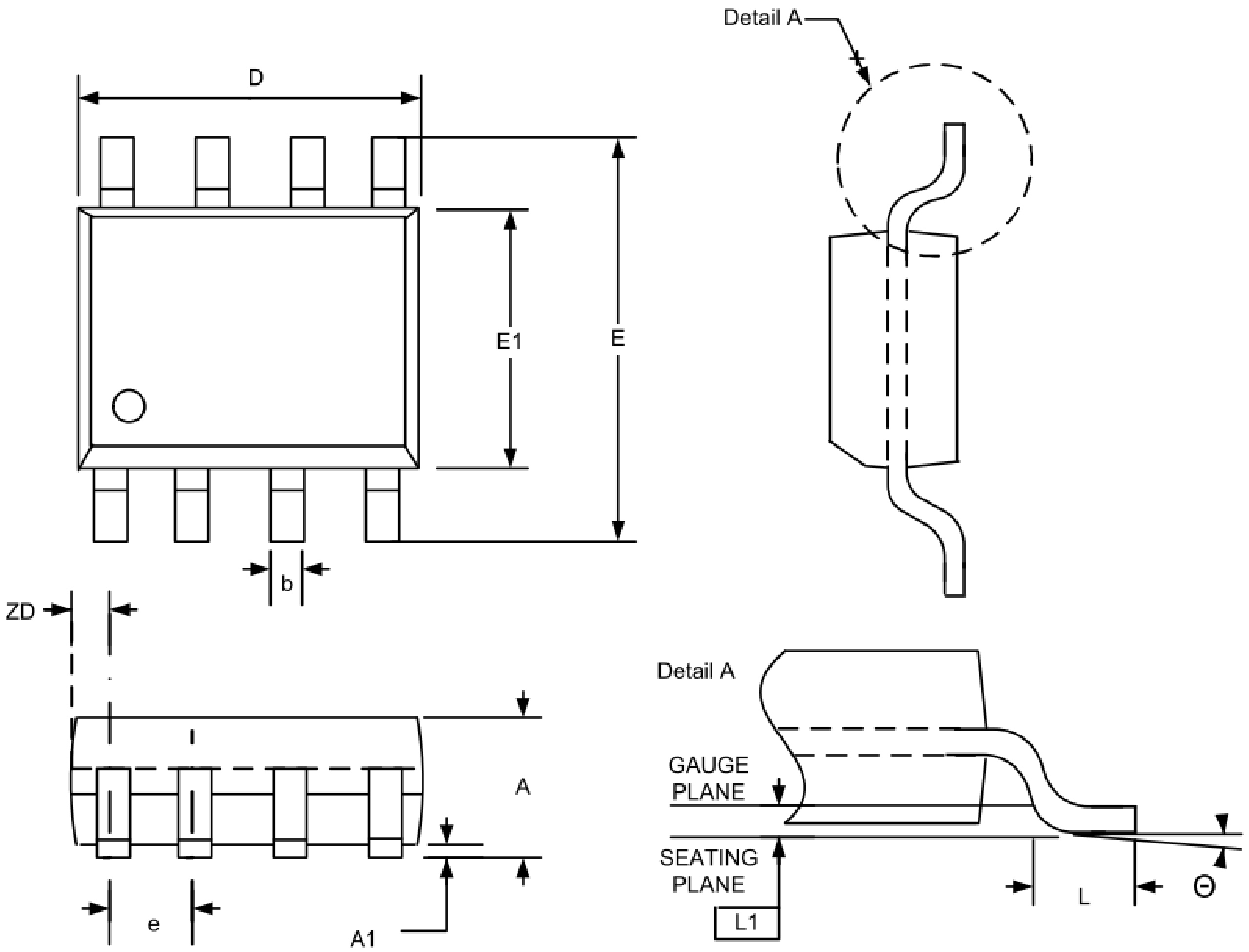
Figure 10. Sanllen-Key 2nd Order Active High-Pass Filter

Input Offset Cancellation

The EC5732 series opamps use internal chopping stabilized technique to cancel dc offset and flick noise. Since the offset temperature drift is a dc parameter, it is also cancelled by the chopping technique. The amplifier requires approximately 100µs to achieve the specified Vos accuracy.

Package Information

SOP-8L

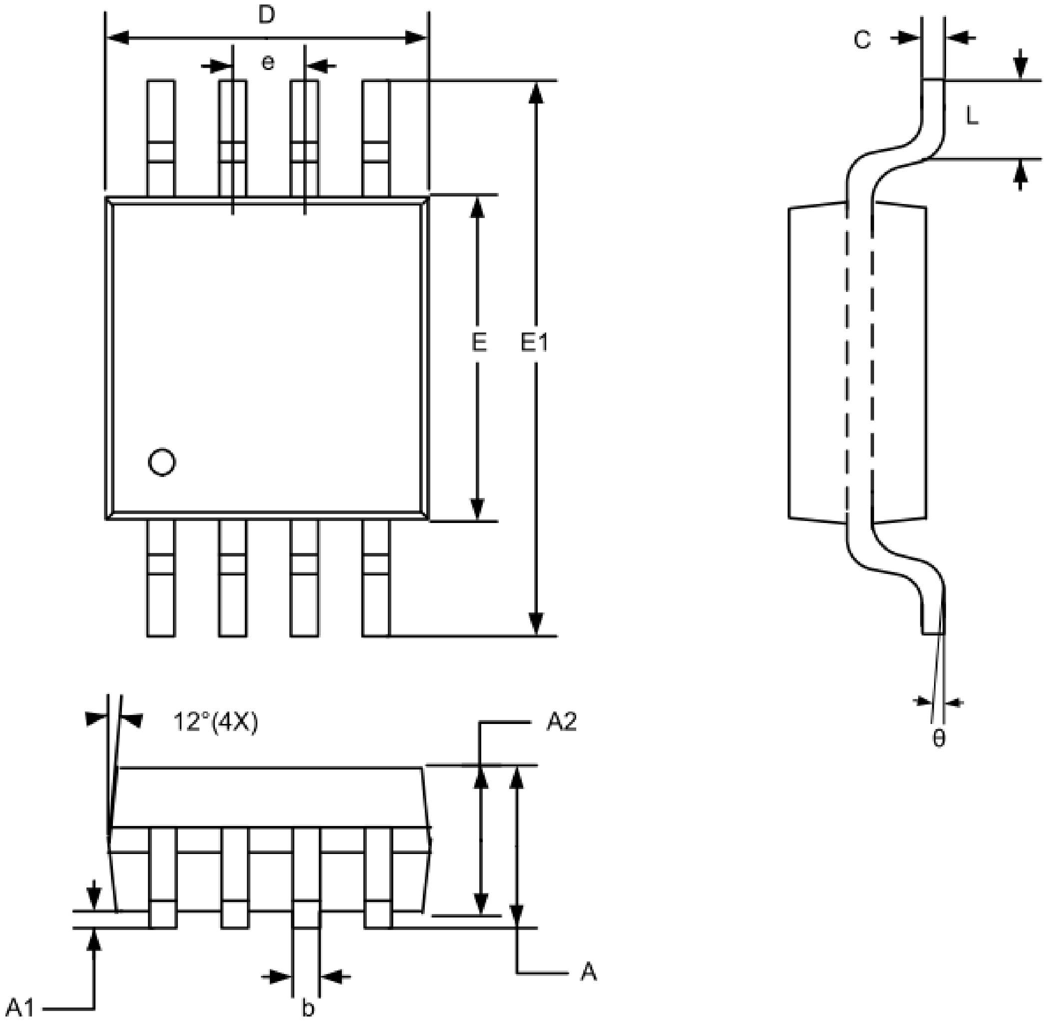


SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.35	--	1.75	0.053	--	0.069
A1	0.10	--	0.25	0.004	--	0.010
b	0.33	--	0.51	0.013	--	0.020
D	4.80	--	5.00	0.189	--	0.197
E	5.80	--	6.20	0.228	--	0.244
E1	3.80	--	4.00	0.150	--	0.157
e	1.27 BSC.			0.050 BSC.		
L	0.38	--	1.27	0.015		0.050
L1	0.25 BSC.			0.010 BSC.		
ZD	0.545 REF.			0.021 REF.		
Θ	0	--	8°	0	--	8°

Note:
1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Dimension b does not include dambar protrusion/intrusion.
4. Refer to Jedec standard MS-012
5. Drawing is not to scale

Package Information

MSOP-8L



SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	--	--	1.10	--	--	0.043
A1	0.05	--	0.15	0.002	--	0.006
A2	0.75	0.85	0.95	0.030	0.033	0.037
b	0.25	--	0.40	0.010	--	0.016
C	0.13	--	0.23	0.005	--	0.009
D	2.90	3.00	3.10	0.114	0.118	0.122
E	2.90	3.00	3.10	0.114	0.118	0.122
E1	4.90 BSC			0.193 BSC		
e	0.65 BSC			0.026 BSC		
L	--	--	0.55	--	--	0.022
Θ	0	--	7°	0	--	7°

Note:
1. Controlling Dimension:MM
2. Dimension D and E1 do not include Mold protrusion
3. Refer to Jedec standard MO187
4. Drawing is not to scale