

Description

These N+P dual Channel enhancement mode power field effect transistors are using trench DMOS technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode.

These devices are well suited for high efficiency fast switching applications.

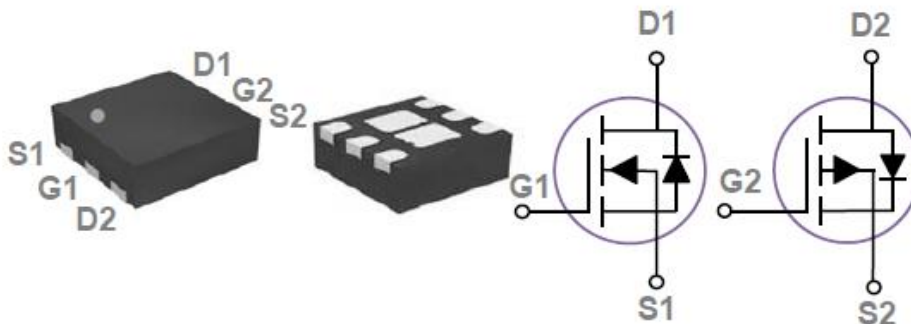
Features

- ◆ 20V/3.8A, $R_{DS(ON)} = 40m\Omega$ @ $V_{GS} = 4.5V$
- ◆ -20V/-2.5A, $R_{DS(ON)} = 100m\Omega$ @ $V_{GS} = 4.5V$
- ◆ Fast switching speed
- ◆ Suit for 1.8V Gate Drive Applications
- ◆ DFN 2x2-6 package design

Applications

- ◆ Notebook
- ◆ Newworking
- ◆ Load Switch
- ◆ Hand-held Instruments

Pin Configuration



Absolute Maximum Ratings ($T_C=25^\circ C$ Unless Otherwise Noted)

Parameter		Symbol	N-Channel	P-Channel	Unit
Drain-Source Voltage		V_{DS}	20	-20	V
Gate-Source Voltage		V_{GS}	± 10	± 10	V
Continuous Drain Current	$T_C=25^\circ C$	I_D	3.8	-2.5	A
	$T_C=100^\circ C$		2.3	-1.5	
Pulsed Drain Current ¹		I_{DM}	15.2	-10	A
Power Dissipation	$T_C=25^\circ C$	P_D	1.25	1.25	W
	Derate above $25^\circ C$		0.01	0.01	W/ $^\circ C$
Operating Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150		$^\circ C$



Thermal Resistance Ratings

Thermal Resistance	Symbol	Typ.	Maximum	Unit
Maximum Junction-to-Ambient	R _{θJA}	-	100	°C/W
Maximum Junction-to-Case	R _{θJC}	-	15	°C/W

Ordering Information

Device	Package	Remark
ECDB2116S	DFN2x2-6	

Note

1. Repetitive Rating : Pulsed width limited by maximum junction temperature.
2. The data tested by pulsed , pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.
3. Essentially independent of operating temperature



Electrical Characteristics ($T_J=25^{\circ}\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Conditions	Limits				Unit
			Ch	Min	Typ	Max	
Static							
Drain-Source Breakdown Voltage	BV_{DSS}	$V_{GS}=0V, I_D=250\mu A$	N	20	-	-	V
		$V_{GS}=0V, I_D=-250\mu A$	P	-20	-	-	
Gate-Threshold Voltage	$V_{GS(th)}$	$V_{GS} = V_{DS}, I_D = 250 \mu A$	N	0.3	0.6	1	V
		$V_{GS} = V_{DS}, I_D = -250 \mu A$	P	-0.3	-0.6	-1	
Gate-Body Leakage	I_{GSS}	$V_{GS} = \pm 10V, V_{DS} = 0V$	N	-	-	± 100	nA
		$V_{GS} = \pm 10V, V_{DS} = 0V$	P	-	-	± 100	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 20V, V_{GS} = 0V, T_J=25^{\circ}\text{C}$	N	-	-	1	uA
		$V_{DS} = -20V, V_{GS} = 0V, T_J=25^{\circ}\text{C}$	P	-	-	-1	
		$V_{DS} = 16V, V_{GS} = 0V, T_J=125^{\circ}\text{C}$	N	-	-	10	
		$V_{DS} = -16V, V_{GS} = 0V, T_J=125^{\circ}\text{C}$	P	-	-	-10	
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 4.5V, I_D = 3A$	N	-	30	40	mΩ
		$V_{GS} = 2.5V, I_D = 2A$		-	42	55	
		$V_{GS} = 1.8V, I_D = 1.5A$		-	55	70	
		$V_{GS} = -4.5V, I_D = -3A$	P	-	82	100	
		$V_{GS} = -2.5V, I_D = -2A$		-	125	140	
		$V_{GS} = -1.8V, I_D = -1A$		-	197	230	
Forward Transconductance	g_{fs}	$V_{DS} = 10V, I_D = 2A$	N	-	4.4	-	S
		$V_{DS} = -10V, I_D = -1A$	P	-	2.2	-	
Diode Forward Voltage	V_{SD}	$I_S = 1A, V_{GS} = 0V, T_J=25^{\circ}\text{C}$	N	-	-	1	V
		$I_S = -1A, V_{GS} = 0V, T_J=25^{\circ}\text{C}$	P	-	-	-1	
Dynamic							
Total Gate Charge ²³	Q_g	N-Channel $V_{DS}=10V, V_{GS}=4.5V, I_D=3A$	N	-	5.8	10	nC
Gate-Source Charge ²³	Q_{gs}		P-Channel $V_{DS}=-10V, V_{GS}=-4.5V, I_D=-2A$	P	-	4.8	
Gate-Drain Charge ²³	Q_{gd}	N-Channel $V_{DS}=10V, V_{GS}=4.5V, I_D=3A$	N	-	0.6	1.5	
			P-Channel $V_{DS}=-10V, V_{GS}=-4.5V, I_D=-2A$	P	-	0.5	
Input Capacitance	C_{iss}	N-Channel $V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	N	-	315	600	pF
			P-Channel $V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	P	-	1.5	
Output Capacitance	C_{oss}	N-Channel $V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	N	-	1.9	4	
			P-Channel $V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	P	-	350	
Reverse Transfer Capacitance	C_{rss}	N-Channel $V_{DS}=15V, V_{GS}=0V, f=1\text{MHz}$	N	-	50	80	
			P-Channel $V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	P	-	65	
Turn-On Delay Time ²³	$t_{d(on)}$	N-Channel $V_{DD}=10V, V_{GS}=4.5V, I_D=1A, R_{GEN}=25\Omega,$	N	-	2.9	6	nS
			P-Channel $V_{DD}=-10V, V_{GS}=-4.5V, I_D=-1A, R_{GEN}=25\Omega$	P	-	3.5	
Rise Time ²³	t_r	N-Channel $V_{DD}=10V, V_{GS}=4.5V, I_D=1A, R_{GEN}=25\Omega,$	N	-	8.4	16	
			P-Channel $V_{DD}=-10V, V_{GS}=-4.5V, I_D=-1A, R_{GEN}=25\Omega$	P	-	12.6	
Turn-Off Delay Time ²³	$t_{d(off)}$	N-Channel $V_{DD}=10V, V_{GS}=4.5V, I_D=1A, R_{GEN}=25\Omega,$	N	-	19.2	38	
			P-Channel $V_{DD}=-10V, V_{GS}=-4.5V, I_D=-1A, R_{GEN}=25\Omega$	P	-	32.6	
Fall-Time ²³	t_f	N-Channel $V_{DD}=10V, V_{GS}=4.5V, I_D=1A, R_{GEN}=25\Omega,$	N	-	5.6	12	
			P-Channel $V_{DD}=-10V, V_{GS}=-4.5V, I_D=-1A, R_{GEN}=25\Omega$	P	-	8.4	

Typical Characteristics (N-Channel)

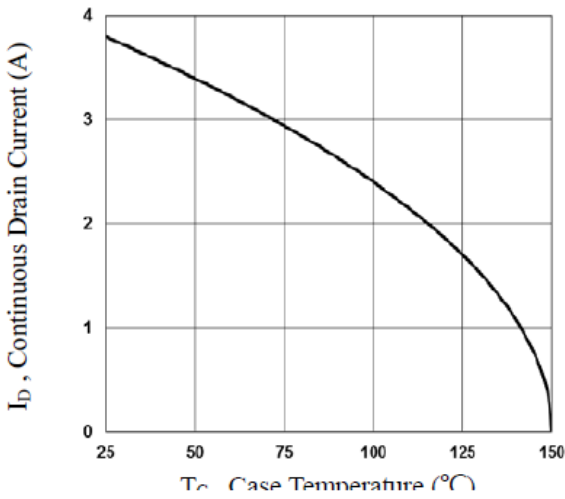


Fig.1 Continuous Drain Current vs. T_c

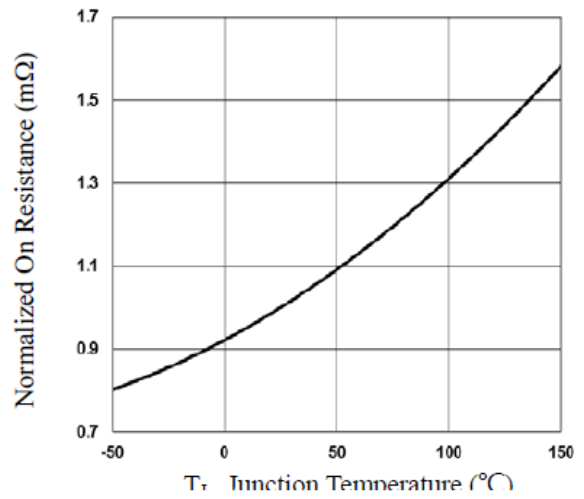


Fig.2 Normalized R_{DS(on)} vs. T_j

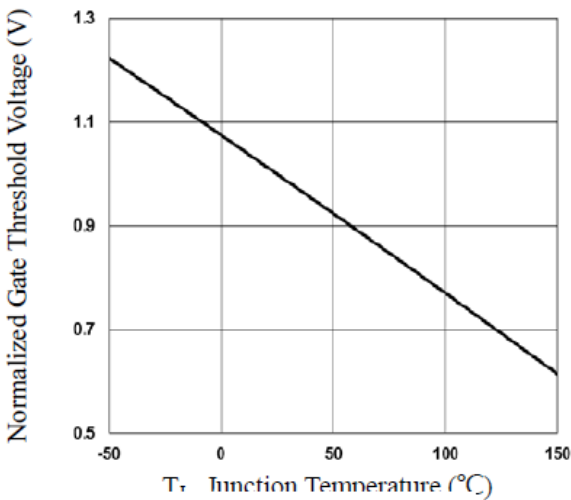


Fig.3 Normalized V_{th} vs. T_j

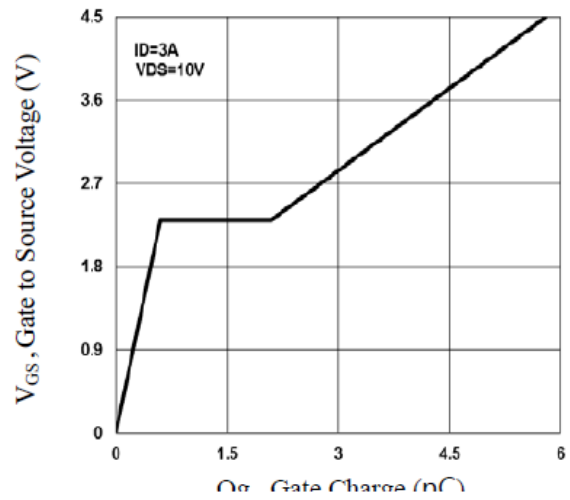


Fig.4 Gate Charge Waveform

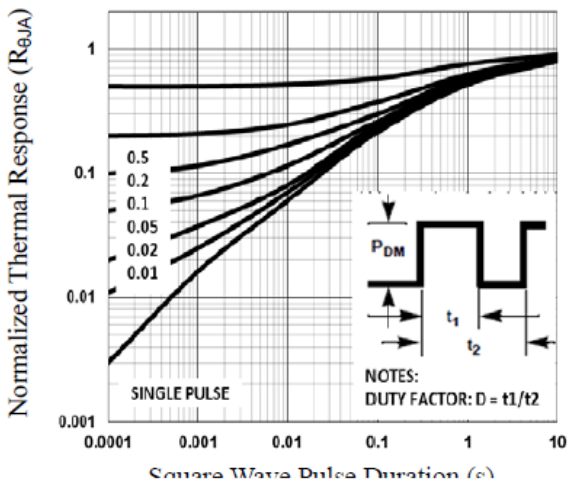


Fig.5 Normalized Transient Impedance

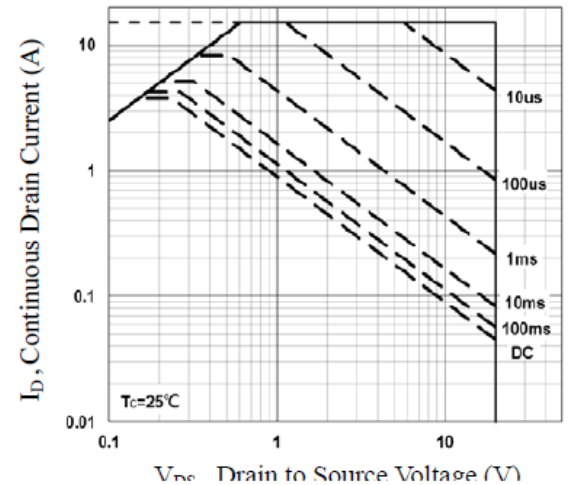


Fig.6 Maximum Safe Operation Area

Typical Characteristics (P-Channel)

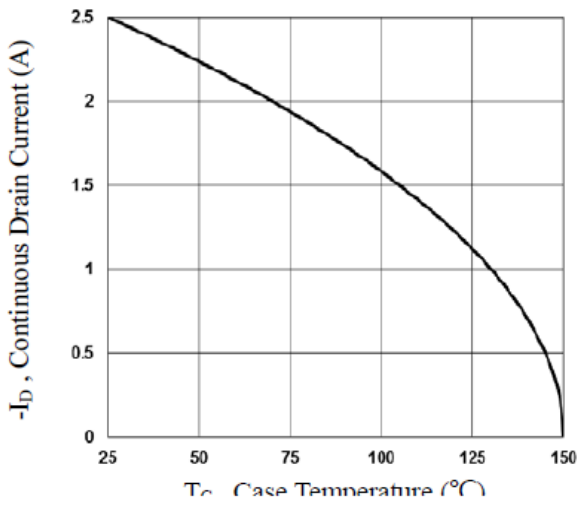


Fig.7 Continuous Drain Current vs. T_c

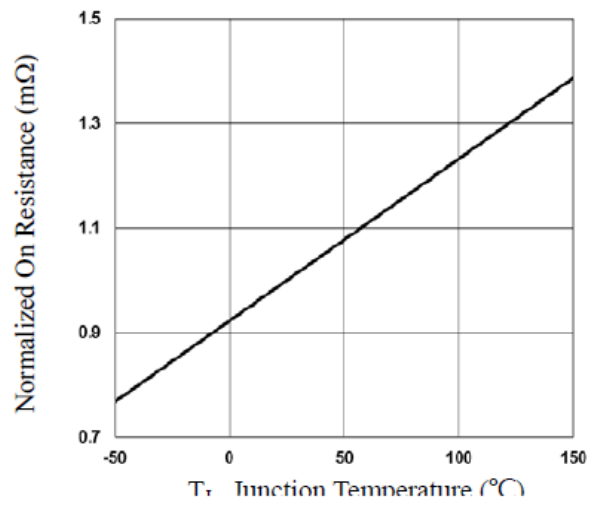


Fig.8 Normalized $R_{DS(on)}$ vs. T_j

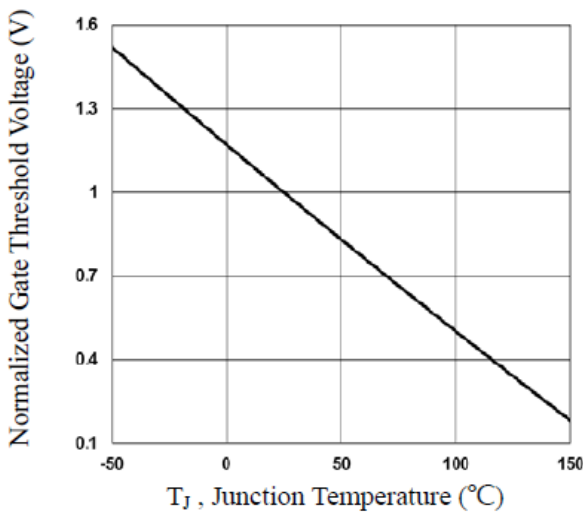


Fig.9 Normalized V_{th} vs. T_j

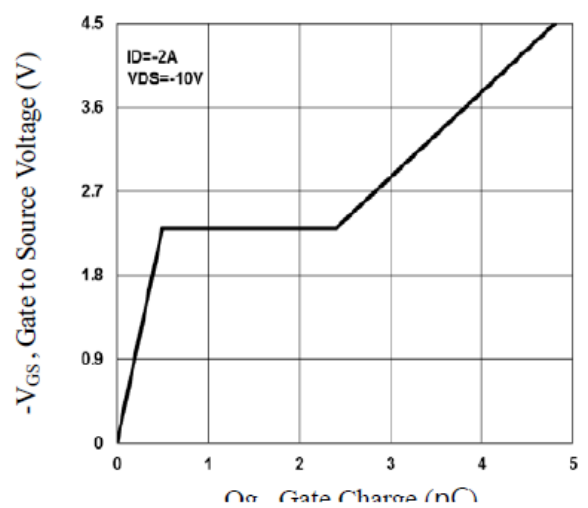


Fig.10 Gate Charge Waveform

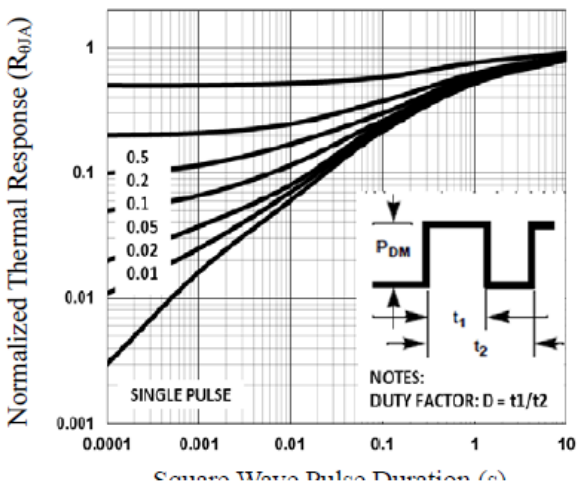


Fig.11 Normalized Transient Impedance

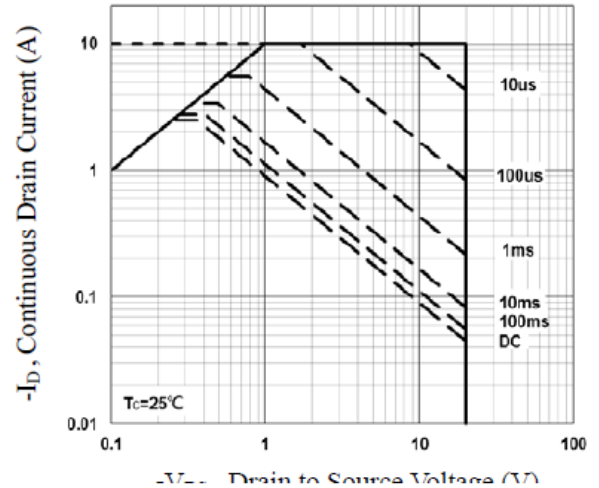
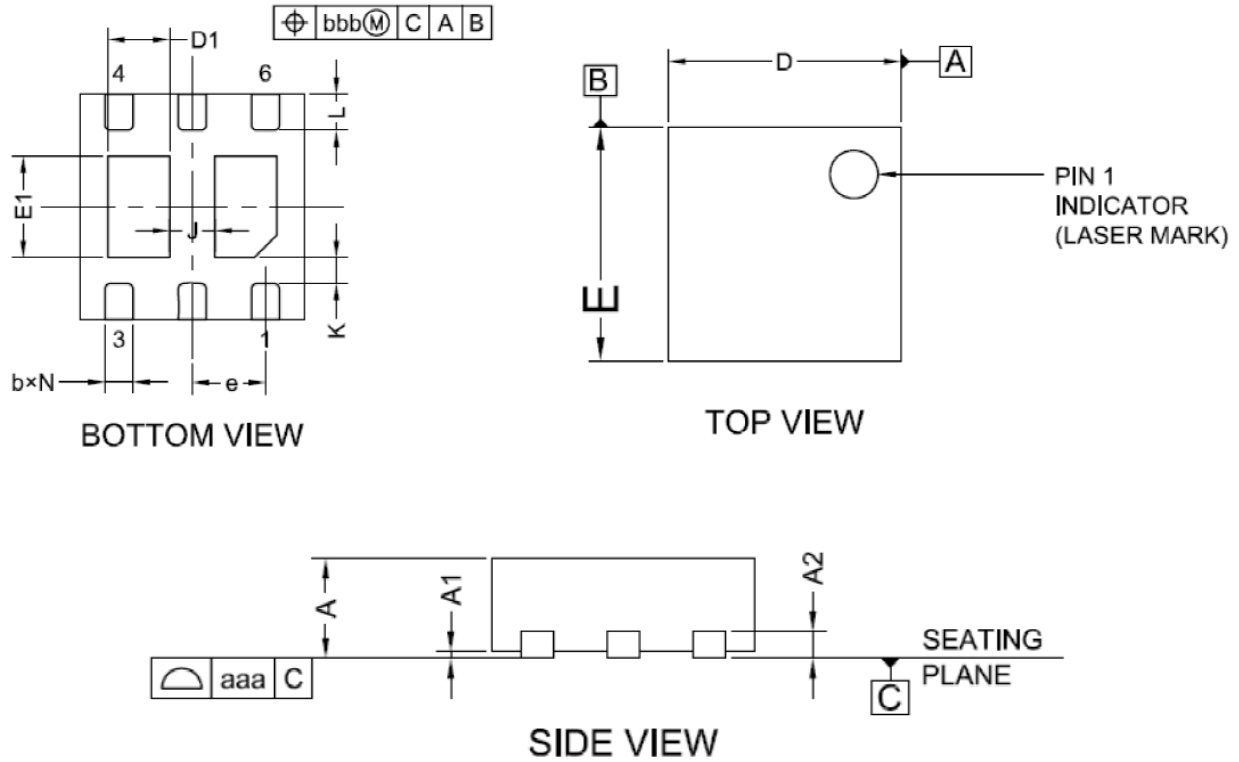


Fig.12 Maximum Safe Operation Area

Physical Dimensions

6-Pin Plastic DFN2x2-6



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	TYP	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A2	0.203		
b	0.20	0.25	0.30
D	1.95	2.00	2.05
D1	0.50	0.55	0.60
E	1.95	2.00	2.05
E1	0.85	0.90	0.95
e	0.65BSC		
L	0.27	0.32	0.37
J	0.40BSC		
K	0.20MIN		
N	6		
aaa	0.08		
bbb	0.10		