General Description

The EC9175 is a simple, cost-effective and high-speed linear regulator designed to generate termination voltage in double data rate (DDR) memory system to comply with the JEDEC SSTL_2 and SSTL_18 or other specific interfaces such as HSTL, SCSI-2 and SCSI-3 etc. devices requirements. The regulator is capable of actively sinking or sourcing up to 2A while regulating an output voltage to within 40mV. The output termination voltage cab be tightly regulated to track 1/2VDDQ by two external voltage divider resistors or the desired output voltage can be programmed by externally forcing the REFEN pin voltage.

The EC9175 also incorporates a high-speed differential amplifier to provide ultra-fast response in line/load transient. Other features include extremely low initial offset voltage, excellent load regulation, current limiting in bi-directions and on-chip thermal shut-down protection. The EC9175 are available in the ESOP8 (Exposed Pad) surface mount packages.

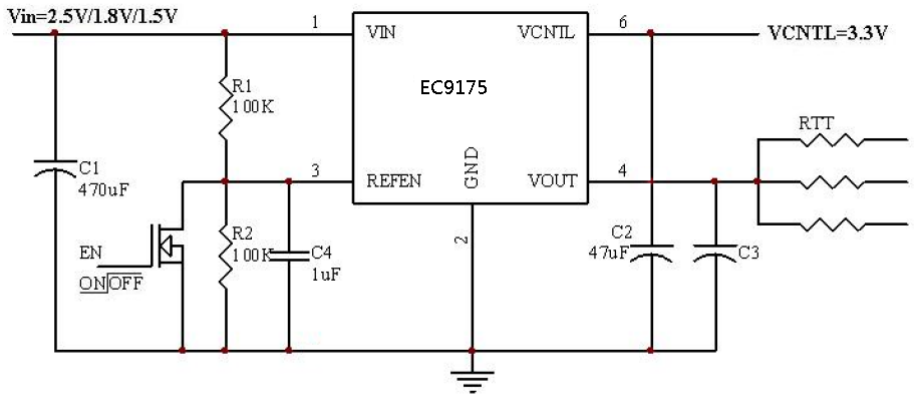
Features

◆Ideal for DDR-I, DDR-II and DDR-III VTT Applications
◆Sink and Source 2A Continuous Current
◆Integrated Power MOSFETs
◆Generates Termination Voltage for SSTL_2, SSTL _18, HSTL, SCSI-2 and SCSI-3 Interfaces.
◆High Accuracy Output Voltage at Full-Load
◆Output Voltage traces REFEN Pin Voltage.
◆Low External Component Count
◆Shutdown for Suspend to RAM (STR) Functionality with High-Impedance Output
◆Current Limiting Protection
◆Thermal Shutdown Protection
◆ESOP-8 with exposed pad Pb-Free Package.

Applications

◆Desktop PCs, Notebooks, and Workstations
◆Graphics Card Memory Termination
◆Set Top Boxes, Digital TVs, Printers
◆Embedded Systems
◆Active Termination Buses
◆DDR-I, DDR-II and DDR-III Memory Systems

Typical application



RTT=50Ω /33Ω /25Ω

C3=10uF (Ceramic) +1000uF under the worst case testing condition

Ordering/Marking Information

EC9175 XX X X

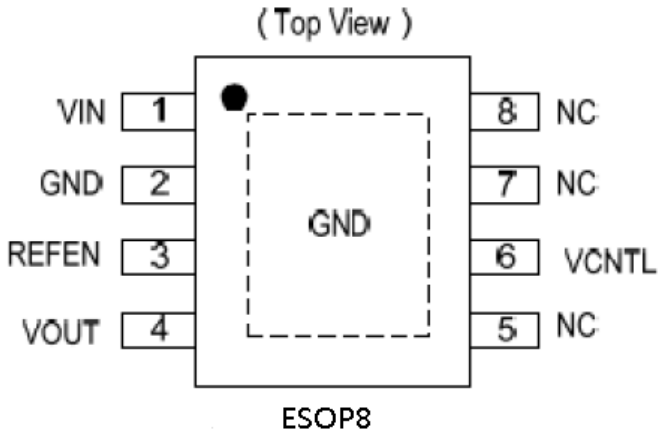
R：Tape & Reel

Package Type：
MH：ESOP8

F：Pb Free
G：Green

Device	Marking	Package	Information
EC9175MHXR	EC9175 LLLLL YYWW	ESOP8	YY: Year code WW: Week code LLLLL: Lot no.

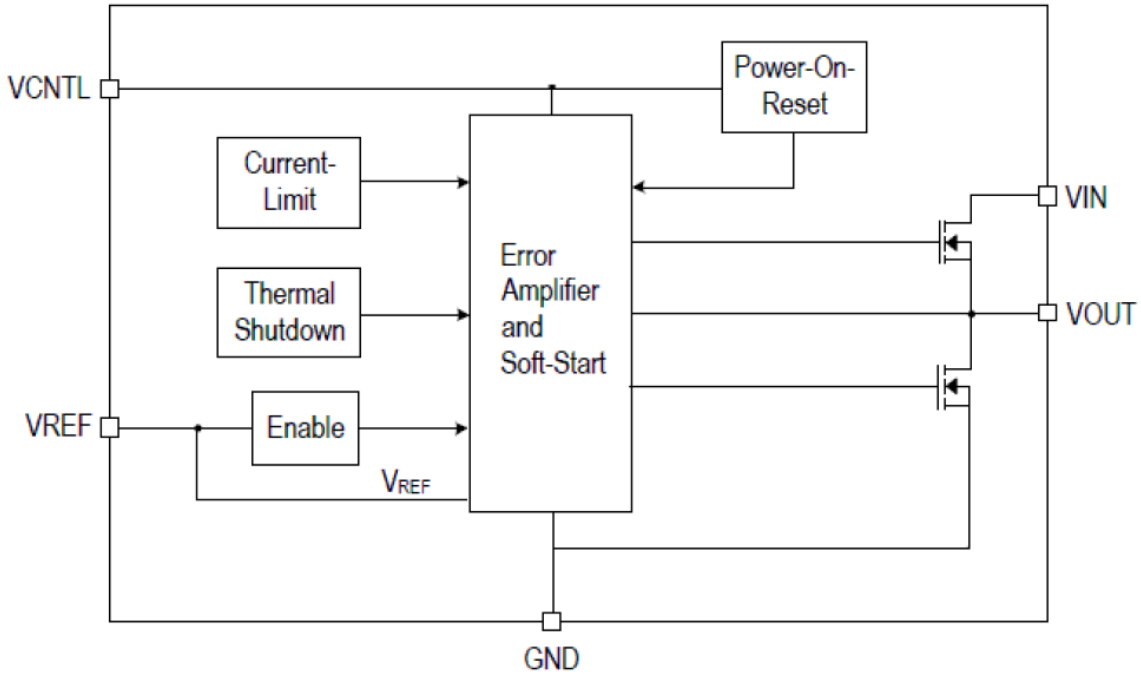
Pin Configurations



Pin Description

NO.	Pin Name	Pin Function Description
1	VIN	Input Voltage pin
2	GND	Ground pin
3	REFEN	Reference voltage input and chip enable pin
4	VOUT	Output Voltage pin
5,7,8	NC	No connect pin
6	VCNTL	Supply Input and Gate drive voltage pin

Functional Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Maximum	Units
VIN	VIN Supply Voltage	6	V
VCNTL	Control Voltage	6	V
PD	Power Dissipation	Internally Limited	W
TST	Storage Temperature Range	-40 to +150	℃
θJC	Thermal Resistance from Junction to case	15	℃/W
θJA	Thermal Resistance from Junction to ambient	40	℃/W

Note:
θJA is measured with the PCB copper area (need connect to Exposed pad) of approximately in1.5 2

Recommended Operating Conditions

Symbol	Parameter	Maximum	Units
VIN	Input Voltage	1.3 to VCNTL	V
VCNTL	Control Voltage	5 or 3.3	V
TA	Ambient Temperature	-40 to +85	℃
TJ	Junction Temperature	-40 to +125	℃

Note:
VOS offset is the voltage measurement defined as VOUT subtracted from VREFEN.

Electrical Characteristics

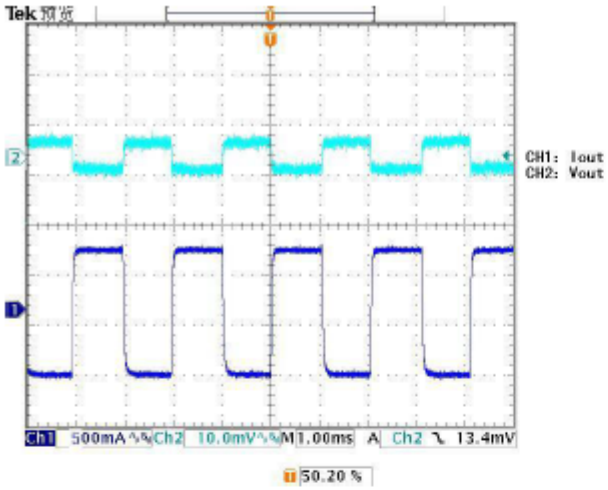
（VIN=2.5V/1.8V/1.5V, VCNTL=3.3V, VREFEN=1.25V/0.9V/0.75V, COUT=10μF (Ceramic), ; Tj=25℃ unless otherwise specified）

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
VCNTL	Gate Drive Voltage Range		-	3.3	5.5	V
VCNTLRTH	POR Threshold		-	2.55	-	V
VCNTL	POR Hysteresis		-	0.1	-	V
VIN	Input Voltage		1.3	-	VCNTL	V
ICNTL	Quiescent Current	IOUT=0A	-	1	3	mA
ISTBY	Standby Current	IOUT=0A, VREFEN=0V	-	1	10	uA
VOS	Output Offset Voltage (Note1)	IOUT=0A	-20	-	+20	mV
△VLOAD	Load Regulation (Note2)	IOUT=±2.0A	-	0.5	±20	%
VIH	Shutdown Threshold	Enable, REFEN Rising	0.65	-	-	V
VIL		Shutdown, REFEN Falling	-	-	0.2	V
ICL-Source	Current Limit	Sourcing	2.1	-	-	A
ICL-Sink		Sinking	2.1	-	-	A
TSS	Soft-Start Period	VOUT=1.25V	-	1.4	-	ms
TSD	Thermal Shutdown		-	155	-	℃
TSDH	Thermal Shutdown Hysteresis		-	30	-	℃

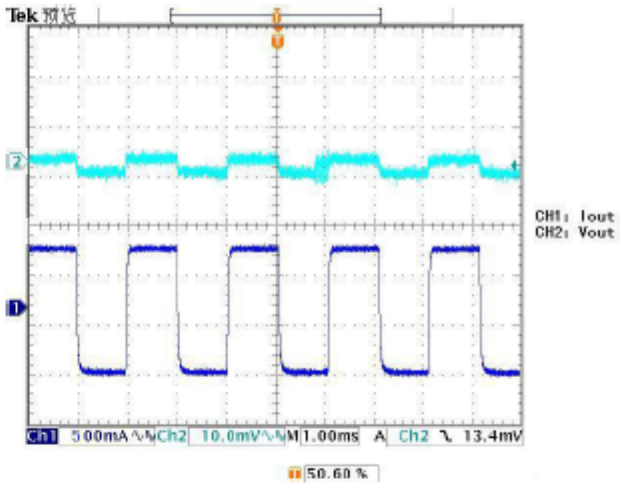
Note 1: VOS offset is the voltage measurement defined as VOUT subtracted from VREFEN.
Note 2: Regulation is measured at constant junction temperature by using a 5ms current pulse. Devices are tested for load regulation in the load range from 0A to 2A.

Typical Performance Characteristics

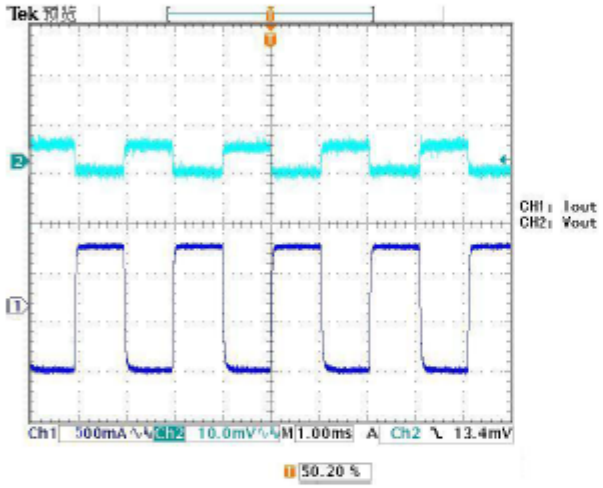
Transient Test



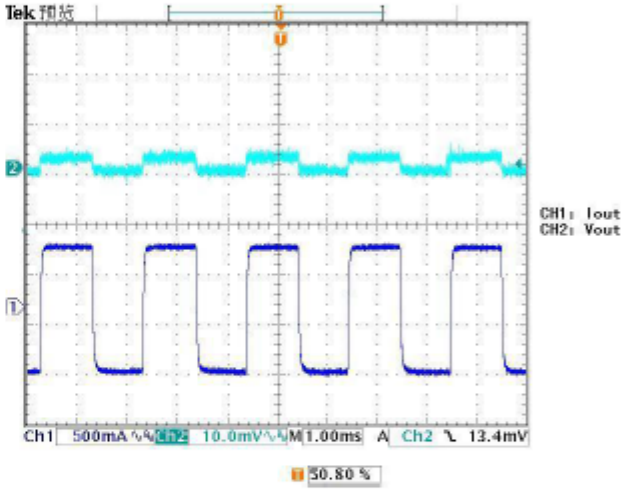
V_{IN}=2.5V, V_{OUT}=1.25V,V_{CNTL}=3.3V, I_{OUT}=1.5A



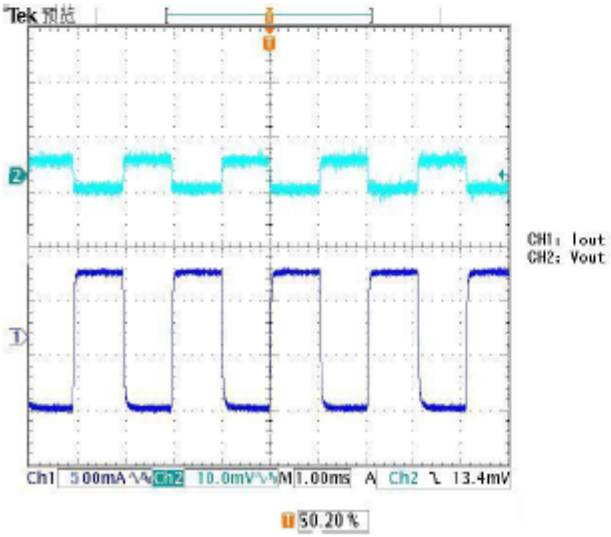
V_{IN}=2.5V, V_{OUT}=1.25V,V_{CNTL}=3.3V, I_{OUT}= -1.5A



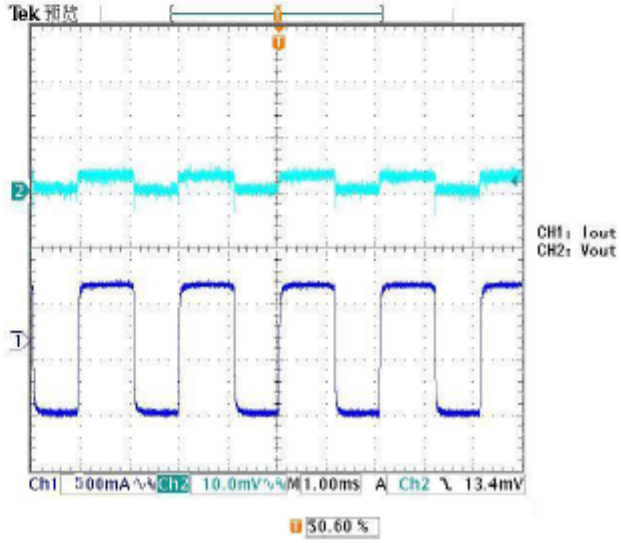
V_{IN}=1.8V, V_{OUT}=0.9V,V_{CNTL}=3.3V, I_{OUT}=1.5A



V_{IN}=1.8V, V_{OUT}=0.9V,V_{CNTL}=3.3V, I_{OUT}= -1.5A



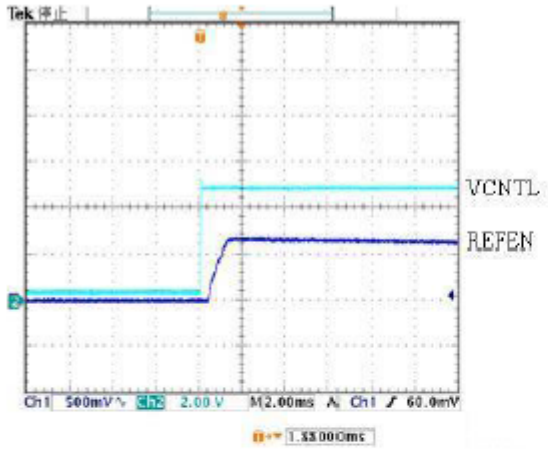
V_{IN}=1.5V, V_{OUT}=0.75V,V_{CNTL}=3.3V,I_{OUT}=1.5A



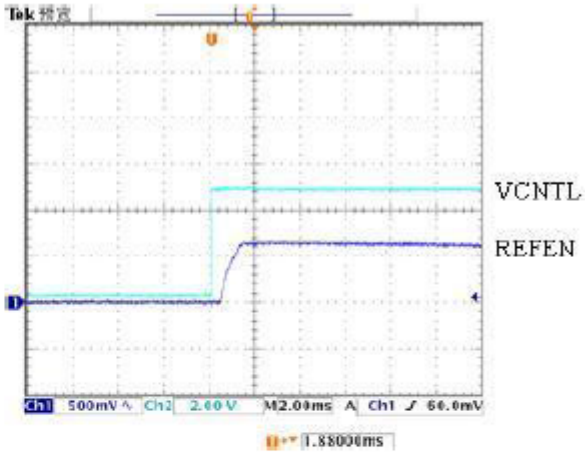
V_{IN}=1.5V, V_{OUT}=0.75V,V_{CNTL}=3.3V,I_{OUT}= -1.5A

Typical Performance Characteristics（continuous）

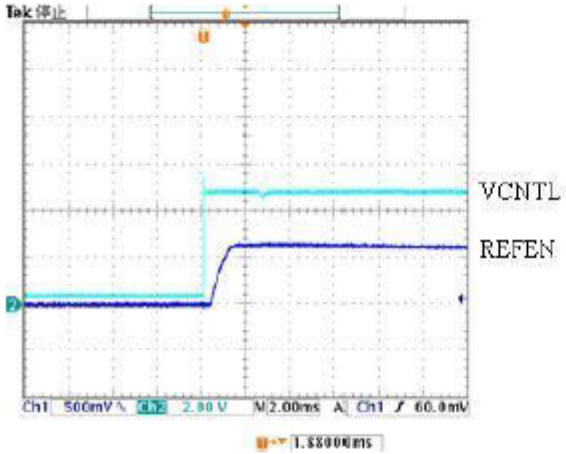
Soft-Start



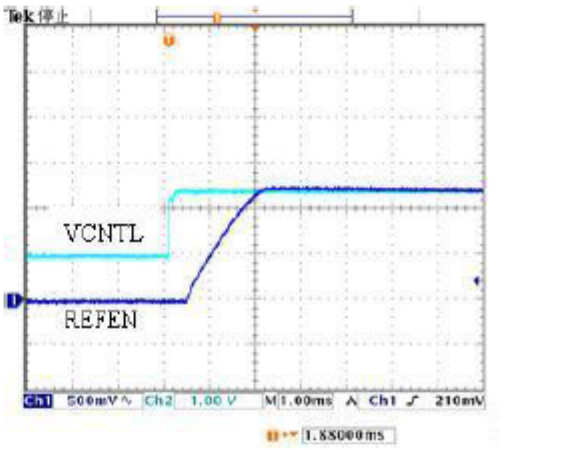
Vin=1.5V,V_{OUT}=0.75V,
I_{OUT}=0mA, V_{CNTL} (3.3V) Power-on



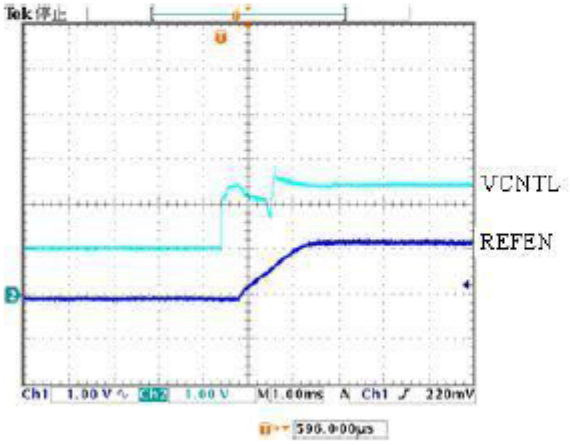
Vin=1.5V,V_{OUT}=0.75V,
I_{OUT}=1A, V_{CNTL} (3.3V) Power-on



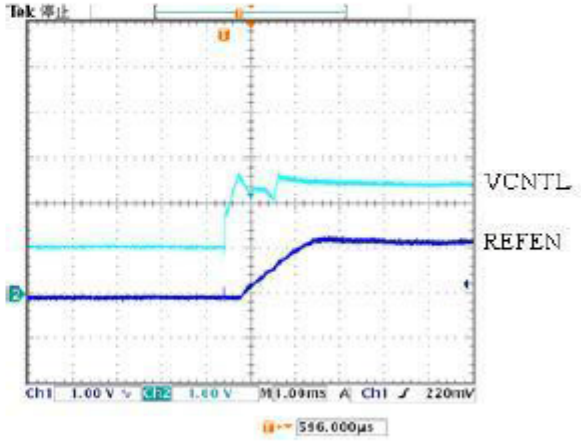
Vin=1.5V,V_{OUT}=0.75V,
I_{OUT}=2A, V_{CNTL} (3.3V) Power-on



Vin(1.5V) Power-on, V_{OUT}=0.75V,
I_{OUT}=0mA, V_{CNTL}= 3.3V

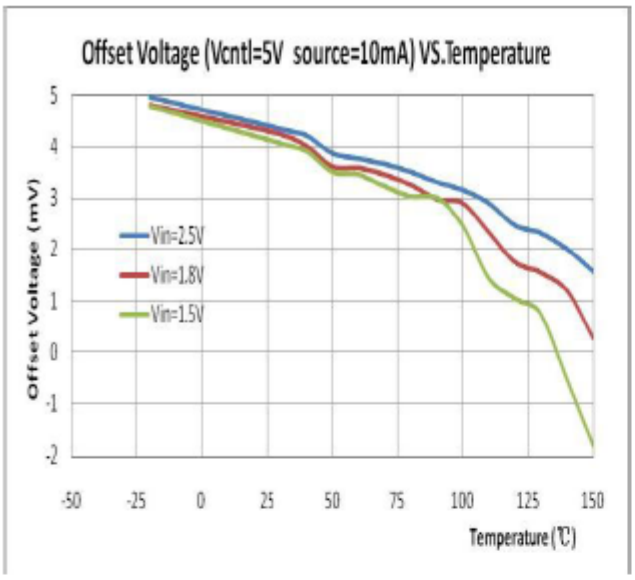


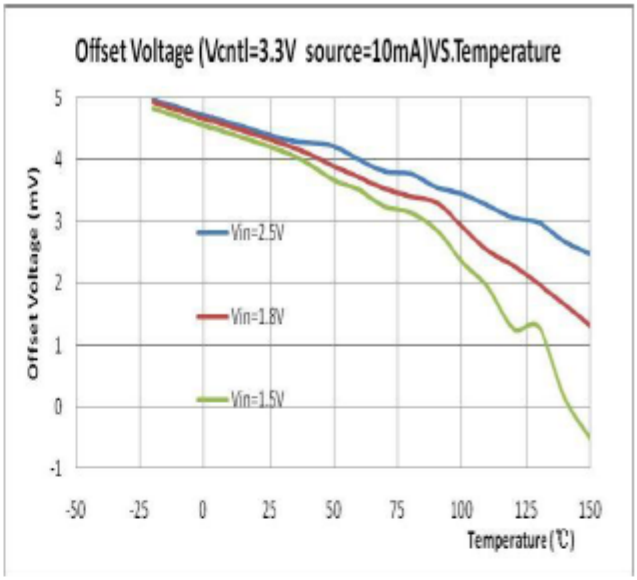
Vin(1.5V) Power-on, V_{OUT}=0.75V,
I_{OUT}=1A, V_{CNTL}=3.3V

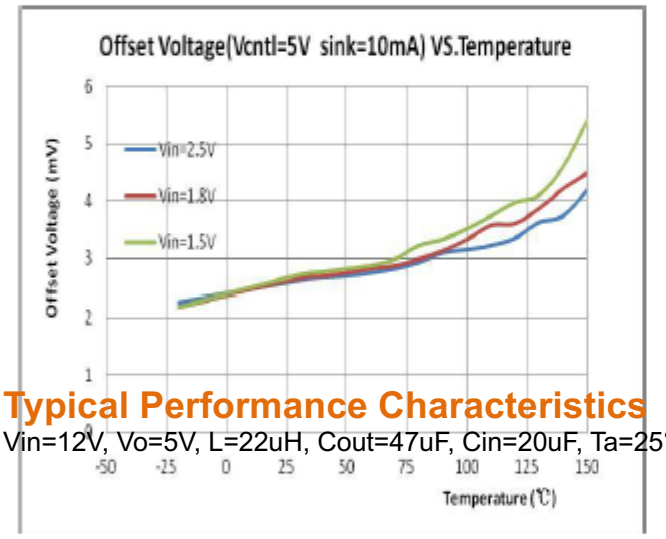


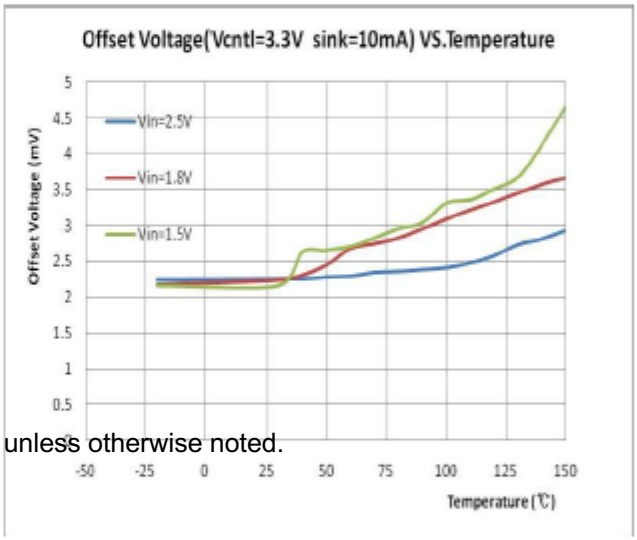
Vin(1.5V) Power-on, V_{OUT}=0.75V,
I_{OUT}=2A, V_{CNTL}=3.3V

Typical Performance Characteristics（continuous）



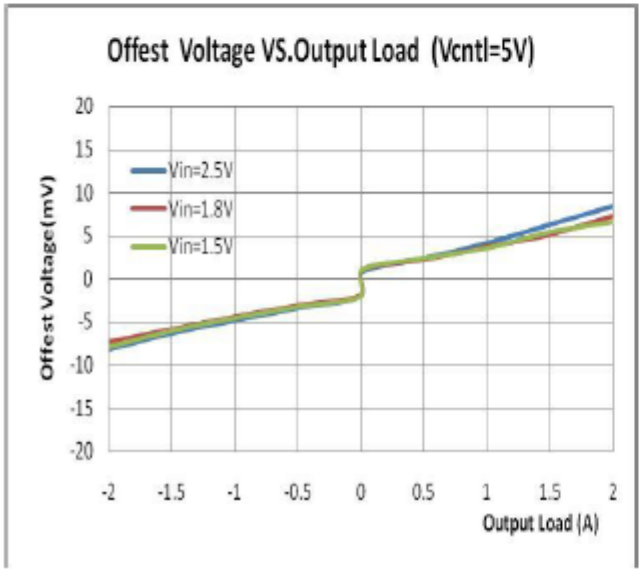


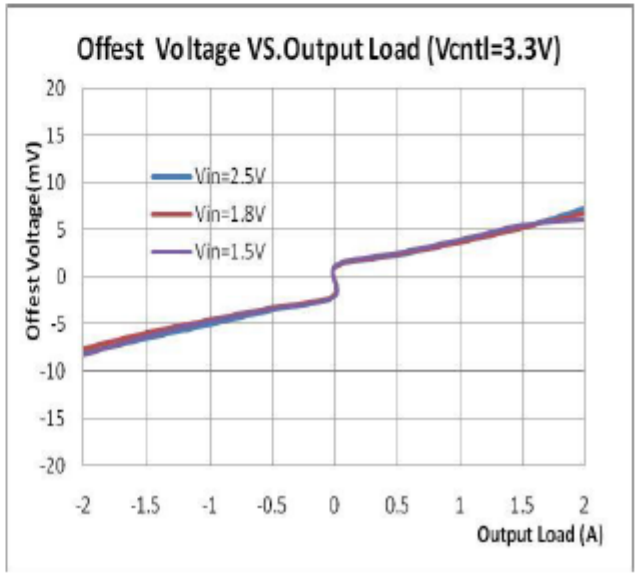




Typical Performance Characteristics

Vin=12V, Vo=5V, L=22uH, Cout=47uF, Cin=20uF, Ta=25°C unless otherwise noted.





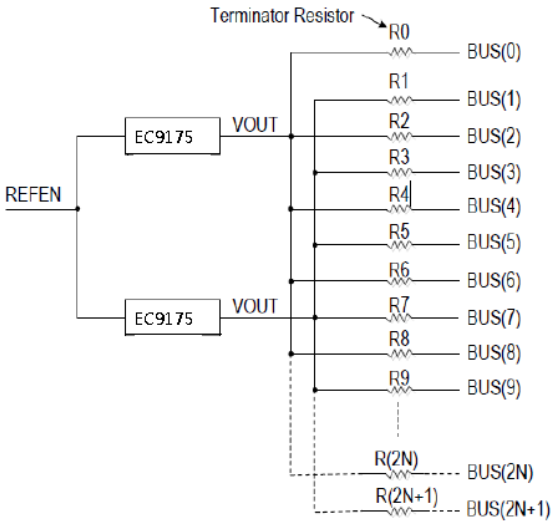
Applications Information

Input Capacitor and Layout Consideration

Place the input bypass capacitor as close as possible to the EC9175. A low ESR capacitor larger than 470uF is recommended for the input capacitor. Use short and wide traces to minimize parasitic resistance and inductance. Inappropriate layout may result in large parasitic inductance and cause undesired oscillation between EC9175 and the preceding power converter.

Consideration while designs the resistance of voltage divider

Make sure the sinking current capability of pull-down NMOS if the lower resistance was chosen so that the voltage on VREFEN is below 0.2V. In addition, the capacitor and voltage divider form the low pass filter. There are two reasons doing this design; one is for output voltage soft-start while another is for noise immunity.



Thermal Considerations

The EC9175 series can deliver a current of up to 2A over the full operating junction temperature range.

However, the maximum output current must be dated at higher ambient temperature to ensure the junction temperature does not exceed 125°C. With all possible conditions, the junction temperature must be within the range specified under operating conditions. Power dissipation can be calculated based on the output current and the voltage drop across regulator. **PD = (VIN - VOUT) × IOUT+ VIN × IQ**

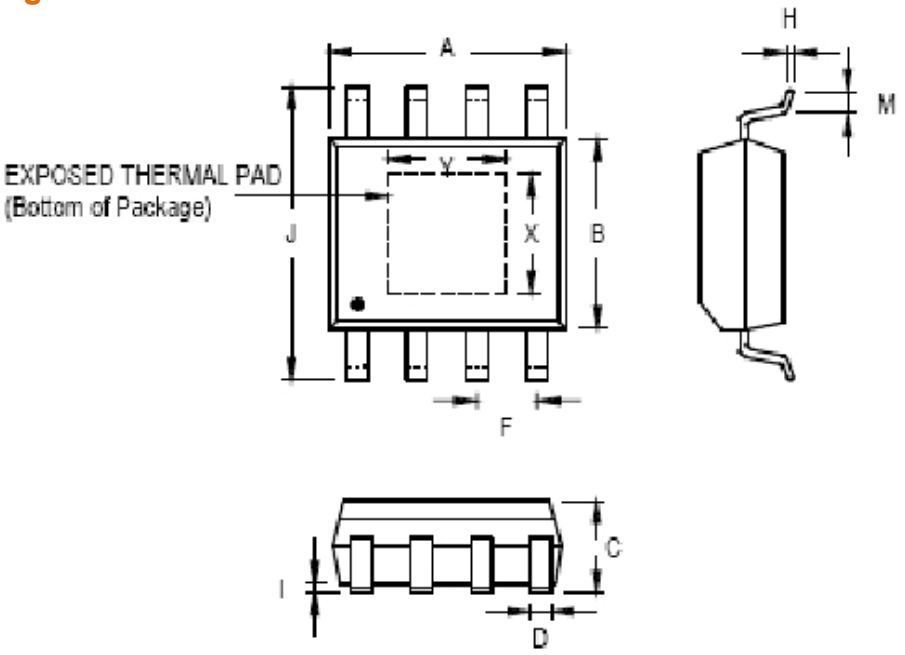
The final operating junction temperature for any set of conditions can be estimated by the following thermal equation:

PD (MAX) = (TJ (MAX) - TA) / θJA

Where TJ(MAX) is the maximum junction temperature of the die (125°C) and TA is the maximum ambient temperature. The junction to ambient thermal resistance (θJA) for ECSOP8 (Exposed pad) package at recommended minimum footprint is 40°C/W on 1.52 and Multi-layer PCB layout. The maximum power dissipation at TA = 25°C can be calculated by following formula: **PD (MAX) = (125°C - 25°C) / 40°C/W =2.5W**

The thermal resistance θJA of ESOP8 (Exposed Pad) is determined by the package design and the PCB design. However, the package design has been decided. If possible, it's useful to increase thermal performance by the PCB design. The thermal resistance can be decreased by adding copper under the expose pad of ESOP8 package. We have to consider the copper couldn't stretch infinitely and avoid the tin overflow.

Outline Drawing For ESOP8



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	4.801	5.004	0.189	0.197
B	3.810	3.988	0.150	0.157
C	1.346	1.753	0.053	0.069
D	0.330	0.508	0.013	0.020
F	1.194	1.346	0.047	0.053
H	0.191	0.254	0.008	0.010
I	0.000	0.152	0.000	0.006
J	5.791	6.198	0.228	0.244
M	0.406	1.270	0.016	0.050
X	2.057	2.515	0.081	0.099
Y	2.057	3.404	0.081	0.134