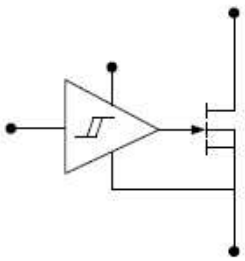
Features

◆650V E-Mode GaN integrated Gate Driver
◆170mΩ RDS_ON
◆Wide input range with hysteresis
◆Wide Vcc range (10V~30V)
◆Fast and controllable rise time and fall time
◆Zero reverse recovery loss
◆Small DFN 5x6 package

DFN 5x6

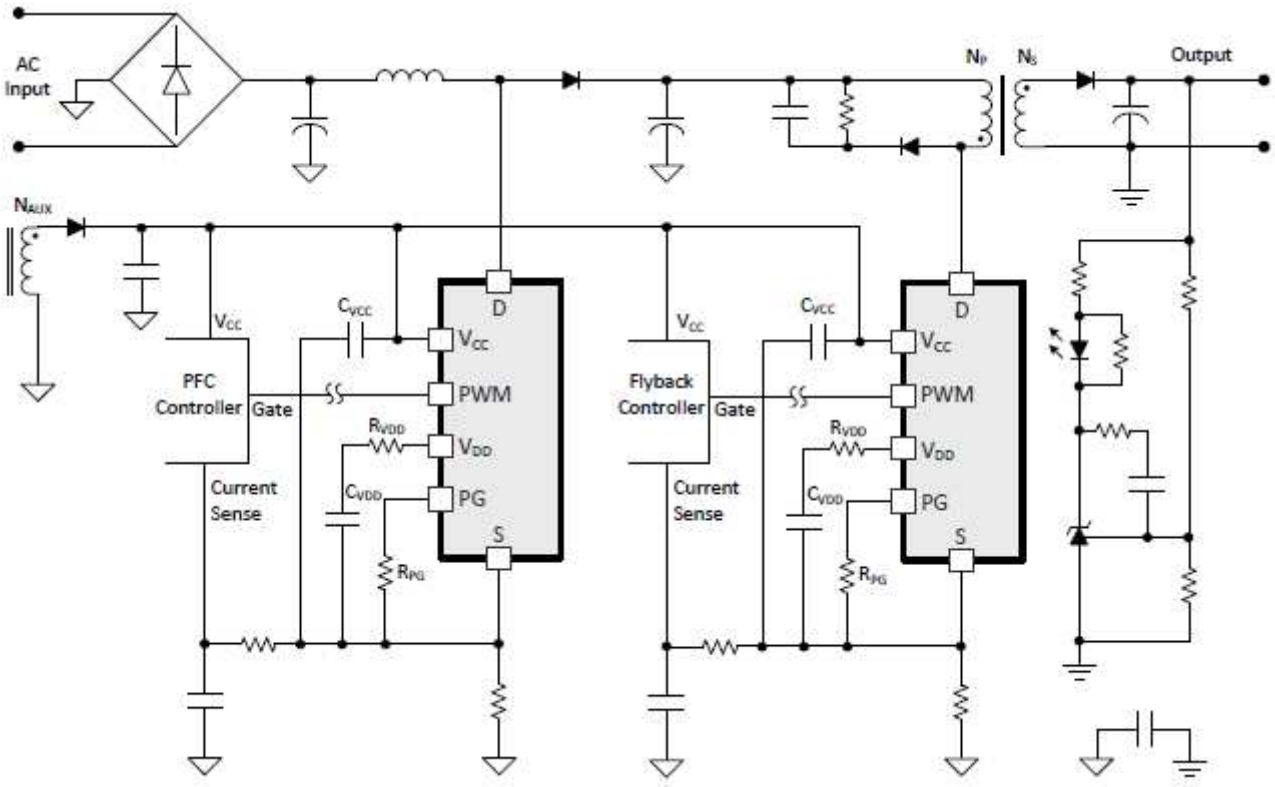
Applications

◆AC-DC Adapter
◆DC-DC Converter
◆LED Lighting
◆Power Factor Correction
◆Charger

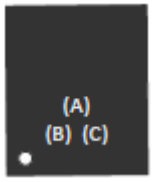


Circuit Symbol

Typical Application Circuit



Marking Information

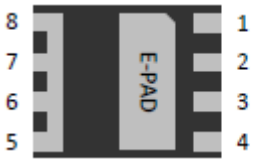


(A) Part Number

(B) – Date Code (Year: 2 digits / Weak: 2 digits)

(C) – Internal Code (3 digits)

Pin Configurations

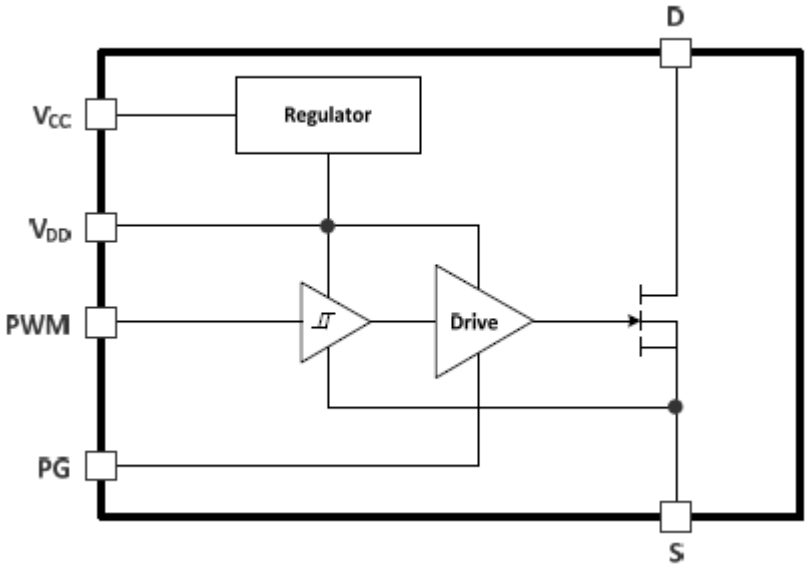


← Bottom view

Pin Assignment

Pin No.	Symbol	Description
1	V_{CC}	Supply voltage.
2	PWM	PWM input.
3	V_{DD}	Gate driver supply voltage. Gate driver turn-on current set pin.
4	PG	Power Ground. Gate driver turn-off current set pin.
5/6/7/8	D	Drain of GaN HEMT.
E-PAD	S	Source of GaN HEMT and Gate Driver ground.

Block Diagram



Absolute Maximum Ratings

Symbol	Parameter	Rating
V_{DS_TRAN}	Transient Drain to Source Voltage (Pulse ≤ 1us)	800V
V_{DS}	Continuous Drain to Source Voltage	650V
V_{CC}	Supply Voltage	30V
V_{PWM}	PWM Pin Voltage	-3V to 30V
I_D	Continuous Drain Current @ T_C=100°C	8A
I_{DP}	Pulsed Drain Current (Pulse = 10us) @ T_C=25°C	16A
	Pulsed Drain Current (Pulse = 10us) @ T_C=125°C	12A
dV/dt	Slew Rate on Drain to Source	200V/ns
T_J	Operating Junction Temperature	-55°C to 150°C
T_{STG}	Storage Temperature	-55°C to 150°C

- These are stress ratings only and functional operation is not implied. Exposure to absolute maximum ratings for prolonged time periods may affect device reliability.
- All voltages are with respect to ground.

Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	10		24	V
V_{PWM}	PWM input Voltage (Do not exceed V_{CC})	0	5	20	V
T_C	Operating Case Temperature	-40		125	°C

- These are conditions under which the device functions but the specifications might not be guaranteed.
- For guaranteed specifications and test conditions, please see the Electrical Specifications.

Package Information

Symbol	Parameter	Rating	Unit
θ_{JC}	Thermal Resistance (Junction to Case)	2	°C/W
θ_{JA}	Thermal Resistance (Junction to Ambient)	38	°C/W

- Thermal resistance is measured on FR4 PCB of 1 square inch 2oz Cu.

Electrical Characteristics

V_{CC}=15V, V_{DS}=400V, F_{SW}=1MHz, R_{TR}=10Ω, T_A=25°C, unless otherwise noted

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{CC} Specifications						
I_Q	V_{CC} Quiescent Current	V_{PWM}=0V		0.06	1.5	mA
I_{CC}	V_{CC} Operating Current	F_{SW}=1MHz, V_{DS}=OPEN		1.1		mA
V_{DD} Specifications						
V_{DD}	V_{DD} Operating Voltage		4.5	5.2	5.9	V
PWM Logic Input Specifications						
V_{PWMH}	PWM Input High Threshold				1.4	V
V_{PWML}	PWM Input Low Threshold		1.1			V
V_{PWM_HYS}	PWM Input Hysteresis			0.3		V
T_{ON}	Turn-on Propagation Delay	Fig. 1 , 2		3		ns
T_{OFF}	Turn-off Propagation Delay	Fig. 1 , 2		4		ns
T_R	V_{DS} Rise Time	Fig. 1 , 2		7		ns
T_F	V_{DS} Fall Time	Fig. 1 , 2		4		ns
Switching Specifications						
F_{SW}	Switching Frequency				2	MHz
T_{PW}	Pulse Width		0.02		1000	us
GaN Specifications						
I_{DSS}	Drain-Source Leakage Current	V_{PWM}=0V, V_{DS}=650V		2	20	uA
		V_{PWM}=0V, V_{DS}=650V, T_J=150°C		10	120	uA
R_{DSON}	Drain-Source Resistance	I_D=3A		170	260	mΩ
		I_D=3A, T_J=150°C		320		mΩ
V_{SD}	Source-Drain Reverse Voltage	V_{PWM}=0V, I_{SD}=2A		2.7		V

Q_{OSS}	Output Charge	V_{PWM}=0V, V_{DS}=400V		19		nC
Q_{RR}	Reverse Recovery Charge			0		nC
C_{OSS}	Output Capacitance	V_{PWM}=0V, V_{DS}=400V		20		pF
$C_{O(ER)}$	Effective Output Capacitance, Energy Related	V_{PWM}=0V, V_{DS}=0V to 400V		27		pF
$C_{O(TR)}$	Effective Output Capacitance, Time Related	V_{PWM}=0V, V_{DS}=0V to 400V		43		pF

- $C_{O(ER)}$ is the fixed capacitance that would give the same stored energy as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}. $C_{O(TR)}$ is the fixed capacitance that would give the same charging time as C_{OSS} while V_{DS} is rising from 0 V to the stated V_{DS}.

Test Circuits

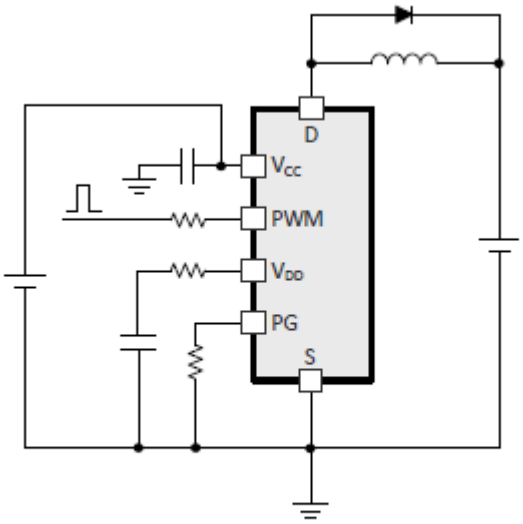


Fig. 1

Inductive switching circuit

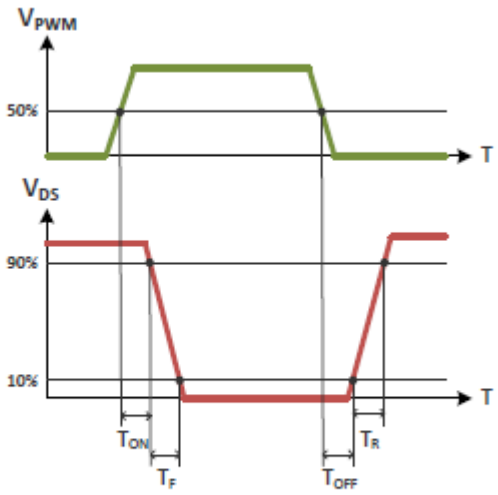


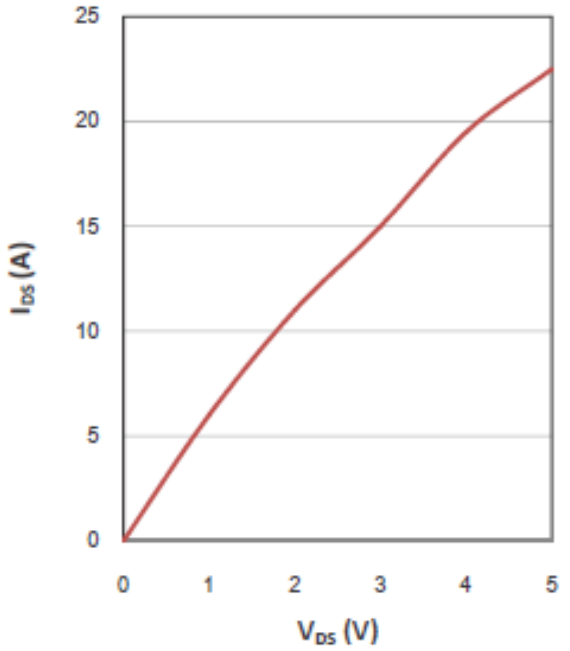
Fig. 2

Propagation delay & rise/fall time definitions

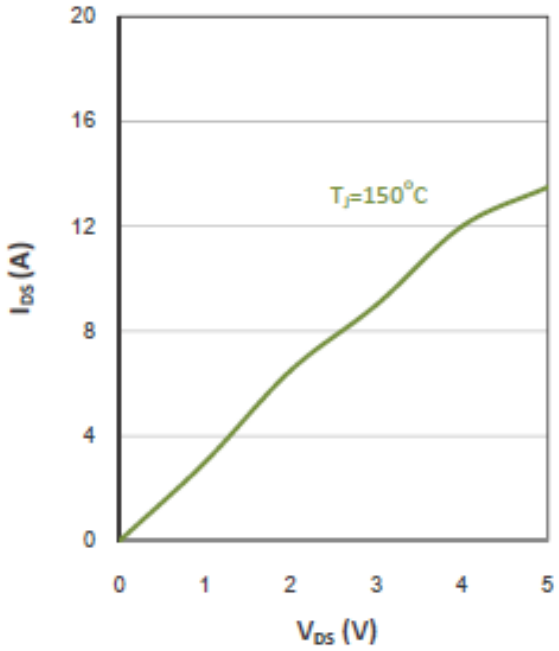
Typical Performance Characteristics

T_J=25°C, unless otherwise noted

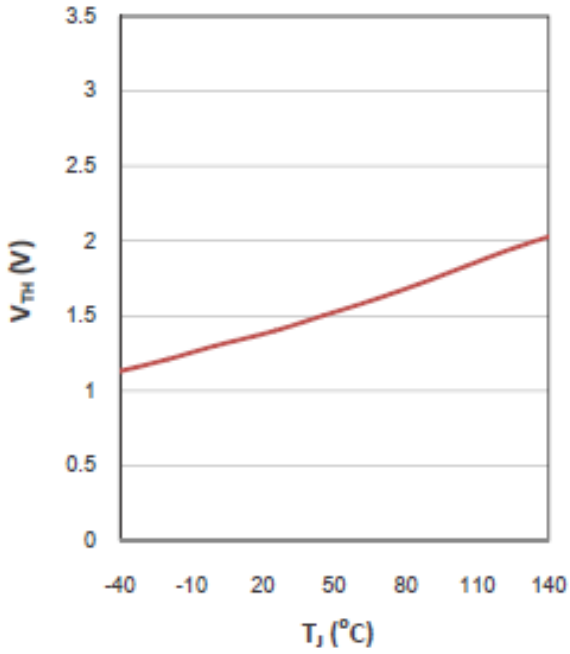
I_{DS} vs. V_{DS}



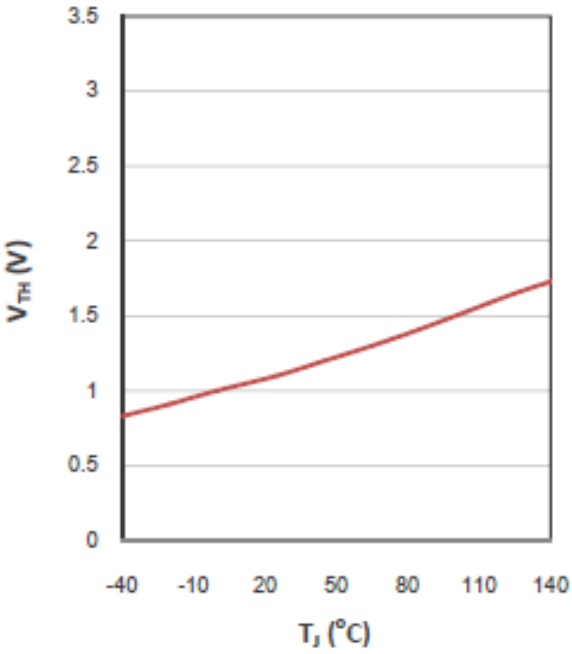
I_{DS} vs. V_{DS}



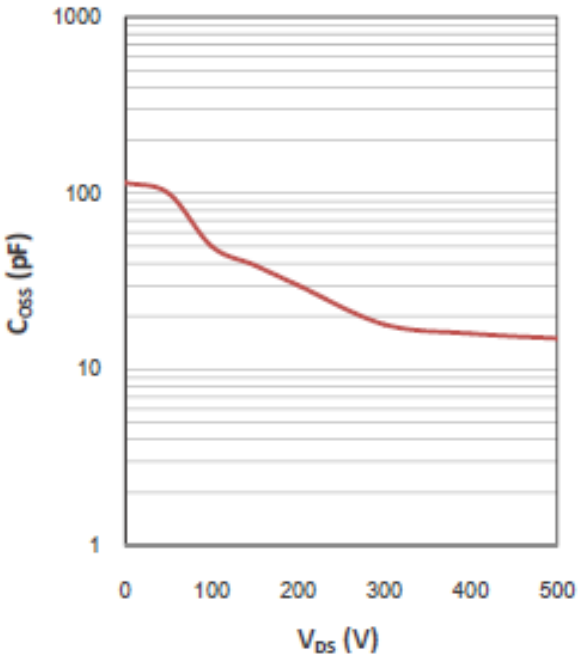
V_{PWMH} vs. Temperature



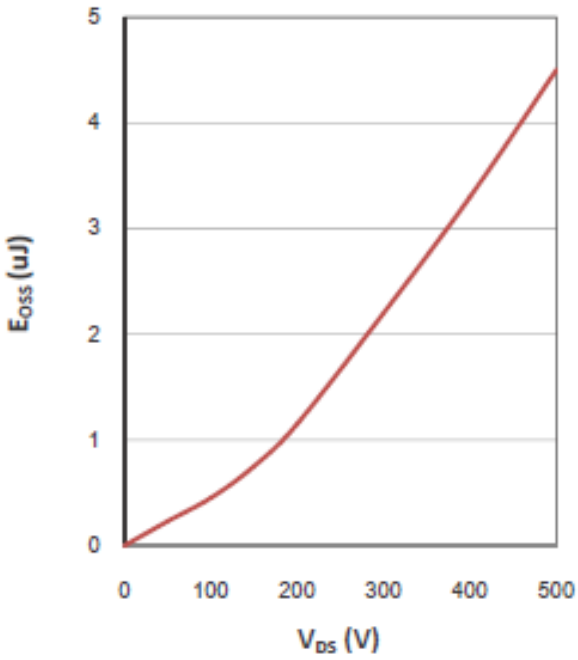
V_{PWML} vs. Temperature



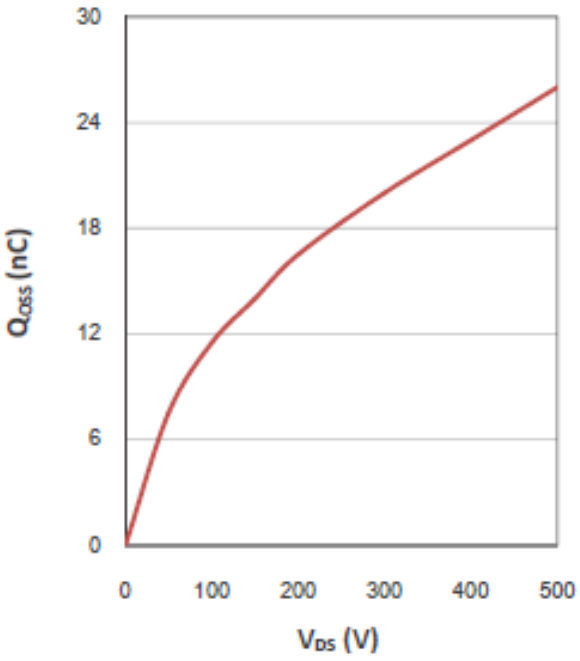
C_{OSS} vs. V_{DS}



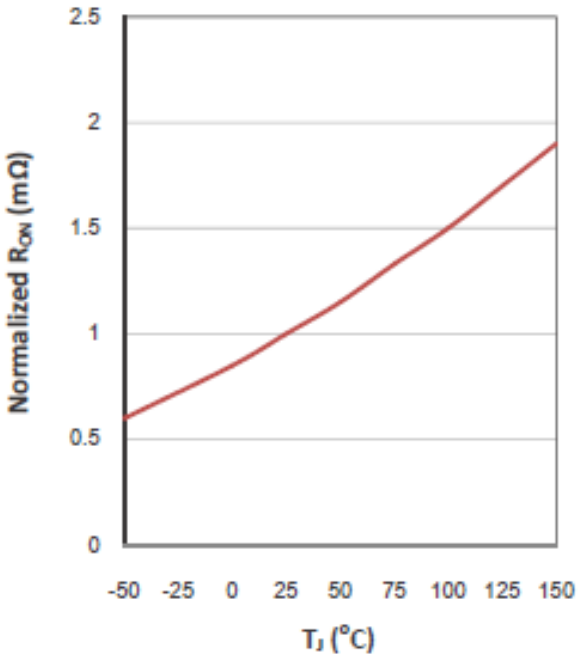
E_{OSS} vs. V_{DS}



Q_{OSS} vs. V_{DS}



Normalized R_{ON} vs. T_J



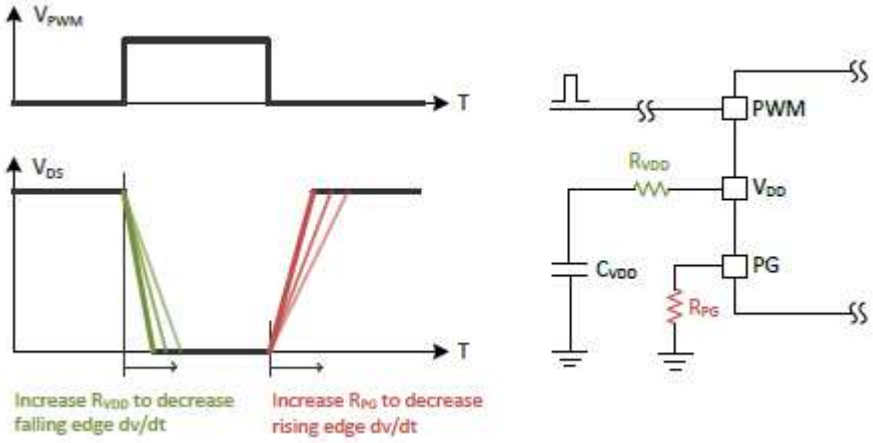
Application Information

Normal Operation

When VCC pin is given a suggestion voltage (10~24V), the internal circuit blocks are active, and the VDD will be set at 5.2V by internal voltage regulator. The internal gate drive detects the PWM signal and according as the PWM voltage level to turn-on/off the GaN HEMT, and the dv/dt slew rate can be set by an external resistor on VDD pin or PG pin. It is useful to optimize the overall efficiency and EMI.

V_{DS} dv/dt Control

Connect an external resistor (R_{VDD}) between V_{DD} pin and C_{VDD} can set the gate driver current that will change the V_{DS} fall time. The V_{DS} rise time can be set by an external resistor (R_{PG}) on PG pin. The following figure shows the V_{DS} dv/dt change with respect to R_{VDD} and R_{PG}.



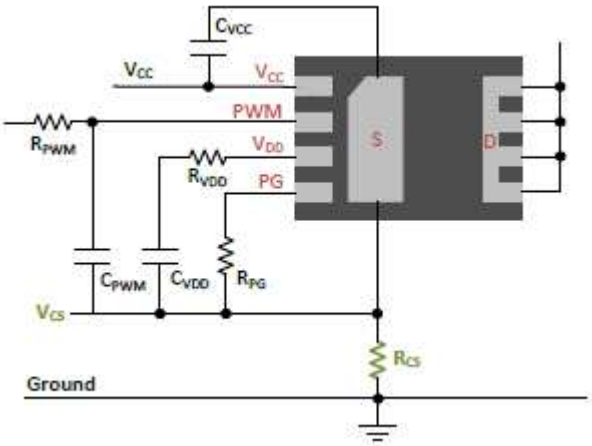
R_{VDD} must be used by minimum 10Ω to ensure application and device robustness.

PWM RC Filter

To prevent the false triggering, an external RC filter can be inserted between the PWM signal and PWM pin to inhibit the high frequency spike and noise. The typical value is 100Ω/100pF.

Current Sensing

Many applications need to sense the current flowing through the power device. A typical connection is placing a current sensing resistor between the Source pin (S) and ground. In this configuration, all of the components around this power device should be grounded to the Source pin (S).



Recommended Component Values

The following table shows the recommended component values for the external C_{VCC}, R_{PWM}, C_{PWM}, R_{VDD}, C_{VDD}, and R_{PG}. These components should be placed as close as possible to the power device. For more layout information, please see the following PCB Layout section.

Symbol	Parameter	Min	Typ	Max	Unit
C_{VCC}	V_{CC} capacitor		0.1		uF
C_{VDD}	V_{DD} capacitor		0.01		uF
R_{VDD}	Gate driver turn-on current set resistor	10	25		Ω
R_{PG}	Gate driver turn-off current set resistor		0		Ω
R_{PWM}	PWM filter resistor		100		Ω
C_{PWM}	PWM filter capacitor		100		pF

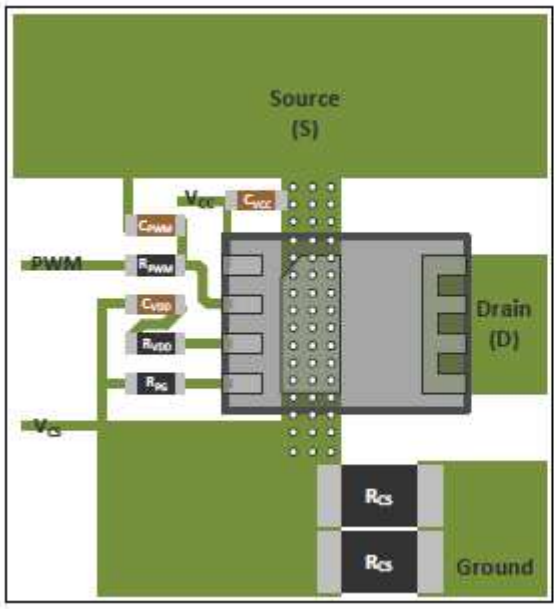
PCB Layout

The design of PCB layout is very important, especially for the switching power supply of high frequency and large peak current. A good layout minimizes EMI on the switching note and current path, and reduces the temperature of power device. The following layout guides can be used to ensure the power device proper operation.

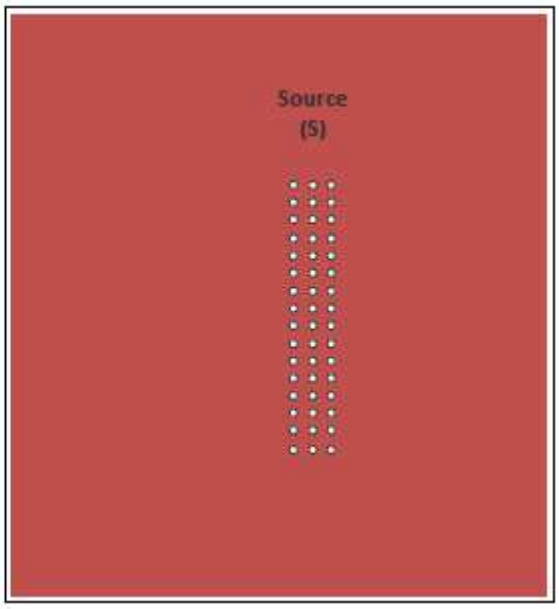
(1). All of the components around the power device should be placed as close as possible, including C_{VCC}, R_{PWM}, C_{PWM}, R_{VDD}, C_{VDD}, and R_{PG}.

(2). Place thermal vias in the source pad to conduct the heat out through the bottom of package and throughthe PCB to the other layers.

(3). For high power density design, use large thermal plane connecting with thermal vias to the source pad and additional PCB layers as much as possible. It is useful to reduce the temperature of power device.



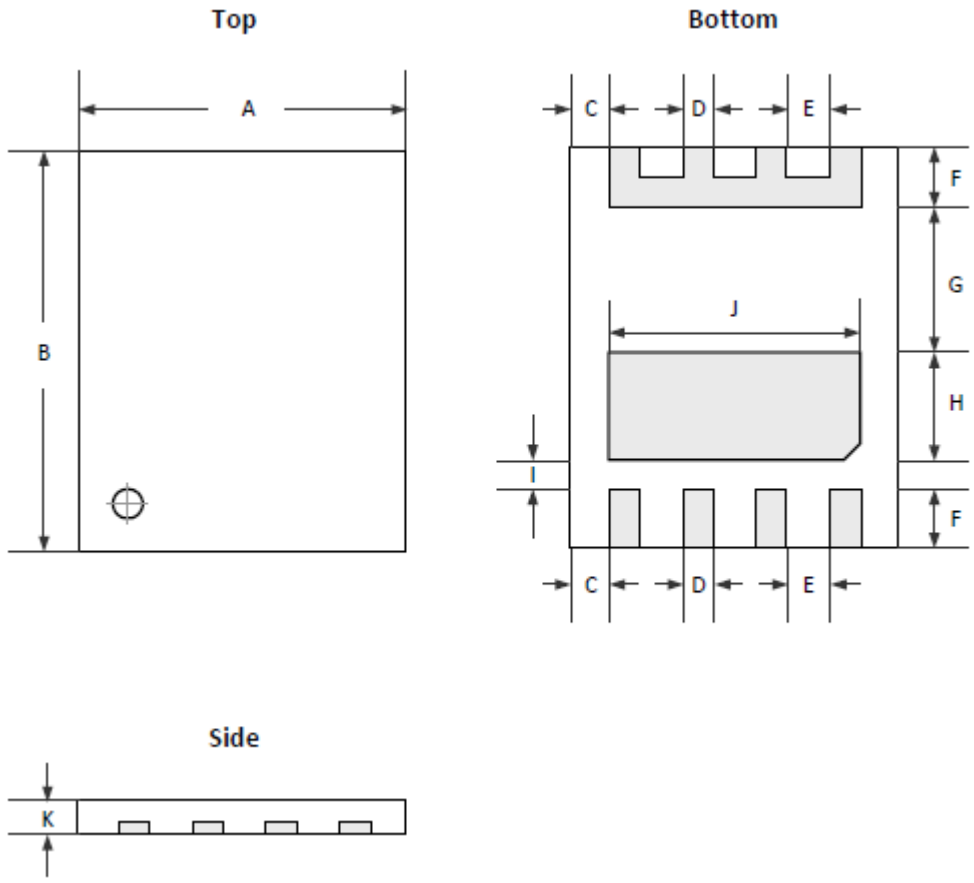
Recommended PCB Layout
(Top)



Recommended PCB Layout
(Bottom)

Package Information

DFN 5x6



Symbol	Dimension (mm)		
	Min.	Typ.	Max.
A	4.9	5	5.1
B	5.9	6	6.1
C	0.245	0.345	0.445
D	0.4	0.5	0.6
E	0.67	0.77	0.87
F	0.6	0.7	0.8
G	1.8	1.9	2
H	2.1	2.2	2.3
I	0.4	0.5	0.6
J	4.2	4.3	4.4
K	0.75	0.85	0.95